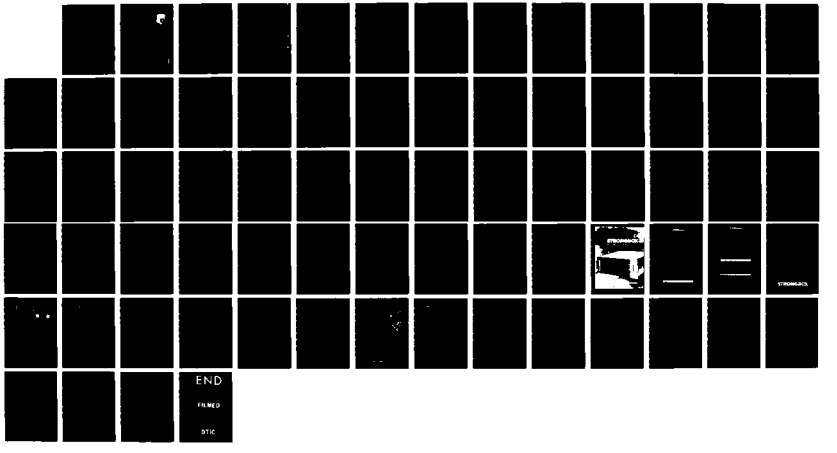
AD-A159 066 DIGITAL SERVOCONTROLLER SYSTEM VOLUME 2 MAINTENANCE MANUAL.. (U) SOUTHWEST RESEARCH INST SAN ANTONIO TX J LOPEZ ET AL. FEB 85 SWRI-14-7676-060-VOL-2 1/1

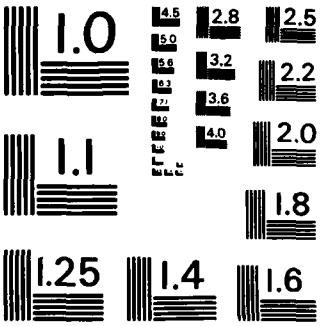
UNCLASSIFIED AFWAL-TR-84-3117-VOL-2 F33615-83-C-3201 F/G 9/2 NL



END

FILMED

DTIC



AFWAL-TR-84-3117
Volume II

DIGITAL SERVOCONTROLLER SYSTEM
VOLUME II - MAINTENANCE MANUAL

Jorge Lopez
Kevin Miller

Southwest Research Institute
San Antonio, Texas

February 1985

Final Report for Period July 1983 to November 1984

FLIGHT DYNAMICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

NOTICE

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture use, or sell any patented invention that may in any way be related thereto.

This report has been reviewed by the Office of Public Affairs (ASD/PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

Nirmal K. Mondol

NIRMAL K. MONDOL
Electrical Engineer

Sanford Lustig

SANFORD LUSTIG
Chief, Structures Test Branch

FOR THE COMMANDER

R J Hegstrom

ROGER J. HEGSTROM, Colonel, USAF
Chief, Structures and Dynamics Division

"If your address has changed, if you wish to be removed from our mailing list, or if the addressee is no longer employed by your organization please notify AFWAL/FIBT, *W-PAFB, OH 45433 to help us maintain a current mailing list".*

Copies of this report should not be returned unless return is required by security considerations, contractual obligations, or notice on a specific document.

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release; distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S): 14-7676-060	5. MONITORING ORGANIZATION REPORT NUMBER(S): AFWAL-TR-84-3117, Vol II
6a. NAME OF PERFORMING ORGANIZATION: Southwest Research Institute; 6b. OFFICE SYMBOL (If applicable):	7a. NAME OF MONITORING ORGANIZATION: Flight Dynamics Laboratory (AFWAL/FIBT)
6c. ADDRESS (City, State and ZIP Code): 6220 Culebra, P.O. Drawer 28510 San Antonio, TX 78284	7b. ADDRESS (City, State and ZIP Code): AF Wright Aeronautical Laboratories Wright-Patterson AFB, OH 45433-6553
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: Flight Dynamics Laboratory; 8b. OFFICE SYMBOL (If applicable): AFWAL/FIBT	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: F33615-83-C-3201
8c. ADDRESS (City, State and ZIP Code): AF Wright Aeronautical Laboratories Wright-Patterson AFB, OH 45433-6553	10. SOURCE OF FUNDING NOS.

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT NO.
62201F	2401	05	17

11. TITLE (Include Security Classification): Digital Servo Controller Final Report, Volume II - Maintenance Manual

12. PERSONAL AUTHOR(S): Lopez, Jorge and Miller, Kevin

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Yr., Mo., Day)	15. PAGE COUNT
Final	FROM 83-7-6 TO 84-11-6	84-8-2 (Vol I)	249

16. SUPPLEMENTARY NOTATION: Volume III contains Software Documentation. Non-DOD requests for this document must be referred to the Flight Dynamics Laboratory, AFWAL/FIBT, WPAFB, OH 45433 and must include a statement of terms and conditions contained in Atch 21 to AFR 300-6.

17. COSATI CODES		
FIELD	GROUP	SUB. GR.

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number): Air frame fatigue tests, load (forces), load control, servocontroller, digital control

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This final report describes an exploratory development effort for the design and fabrication of a digital servocontroller system for load control in full-scale air-frame fatigue tests. Each digital controller replaces four analog controllers. The LSI-11/23 microcomputer in the digital controller executes a PI algarithm to implement direct digital control. It may operate in a stand-alone mode or as a slave processor to a master computer via fiber optic link. Other programmable features specifying loop parameters, building load profiles, adjusting control system gains and monitoring alarm and abort conditions.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☒ DTIC USERS ☐	Unclassified

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE NUMBER (Include Area Code)	22c. OFFICE SYMBOL
Nirmal K. Mondol	513/255/2487	AFWAL/FIBT

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

PREFACE

This is the final report of work accomplished and results achieved at the Experimental Control Group, Structures Test Branch, AFWAL/FIBT, WPAFB, Ohio. The digital servocontroller was developed by Southwest Research Institute, San Antonio, Texas, under Contract F33615-83-C-3201 during the time period July 83 thru November 84.

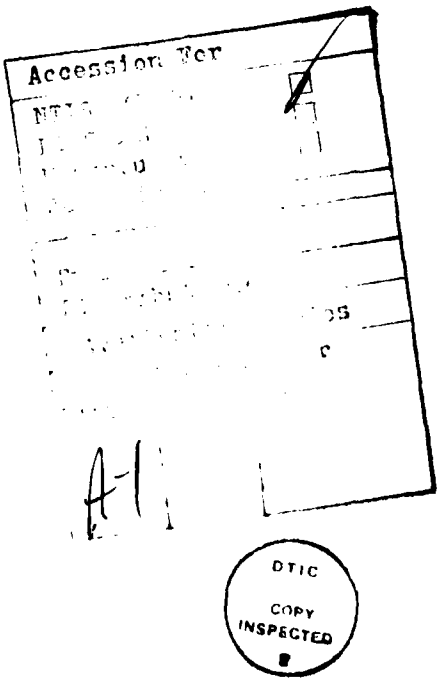


TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The digital servocontroller system was developed by Southwest Research Institute (SwRI) for the Air Force Wright Aeronautical Laboratories. This document provides the information necessary to maintain the digital servocontroller system. A complete description of the system and calibration procedures are provided.

Section 2 lists applicable documents which are referenced in this manual. Section 3 provides a brief description of the servocontroller system. Sections 4 through 8 describe in detail the components of the servocontroller system. Section 9 outlines the system cabling. Section 10 provides detailed procedures for calibrating the servocontroller system.

2.0 APPLICABLE DOCUMENTS

The following is a list of documents which will be referred to in this document which are not included in Appendix A:

(1) Microcomputers and Memories, Digital Equipment Corp., 1982.
(2) Microcomputers Interfaces Handbook, Digital Equipment Corp., 1982.
(3) User Manual for DT2762 Series, Data Translation, Inc., 1979.

3.0 SYSTEM DESCRIPTION

The digital servocontroller system was designed and programmed to function as a general purpose load controller. The system offers various modes of operation and an easy to learn operator interface. The servocontroller system is designed to control one to four channels. A menu driven display guides the operator in performing the different tasks associated with load control tests including: specifying loop parameters, building load profiles, adjusting the control system gains and monitoring alarm and abort conditions. The servocontroller system consists of the following components:

(1) System Enclosure
(2) Microcomputer System
(3) Discrete Interface Card
(4) Signal Conditioning Terminal Panel
(5) Servo Driver Cards
(6) Strain Gauge Signal Conditioning Cards
(7) Fiber-Optic System

Figure 1 shows a simplified block diagram of the system and Figure 2 shows the system and its components along with their respective unit designations. Two serial ports link the microcomputer with the operator. One is used to interface the system terminal (GFE). The terminal is the main operator interface with the system. The operator is able to monitor loop parameters as well as alter them. Control of load profile runs is done through the terminal. This includes building and executing. The other serial port is used to interface the system with a master computer (GFE). The master computer has the ability to generate profiles and download them to the servocontroller system. The servocontroller system interfaces with the hydraulic system through the Signal Conditioning Terminal Panel. Signals from each of the Microcomputer System's digital to analog (D/A) converters are converted into current signals used to drive the servovalves. The feedback signals from the load cells are conditioned to high level signals at the Signal Conditioning Terminal Panel before being measured by the microcomputer system's A/D converters. Discrete signals are provided to the Signal Conditioning Terminal Panel from the servocontroller system via its discrete output lines. The front panel switches interface the servocontroller system through the Discrete Interface Card. Each component is discussed in detail in the following sections. For a complete description of the operating modes and operator interfaces, refer to the Digital Servocontroller System Operator's Manual - Final Report, Volume I.

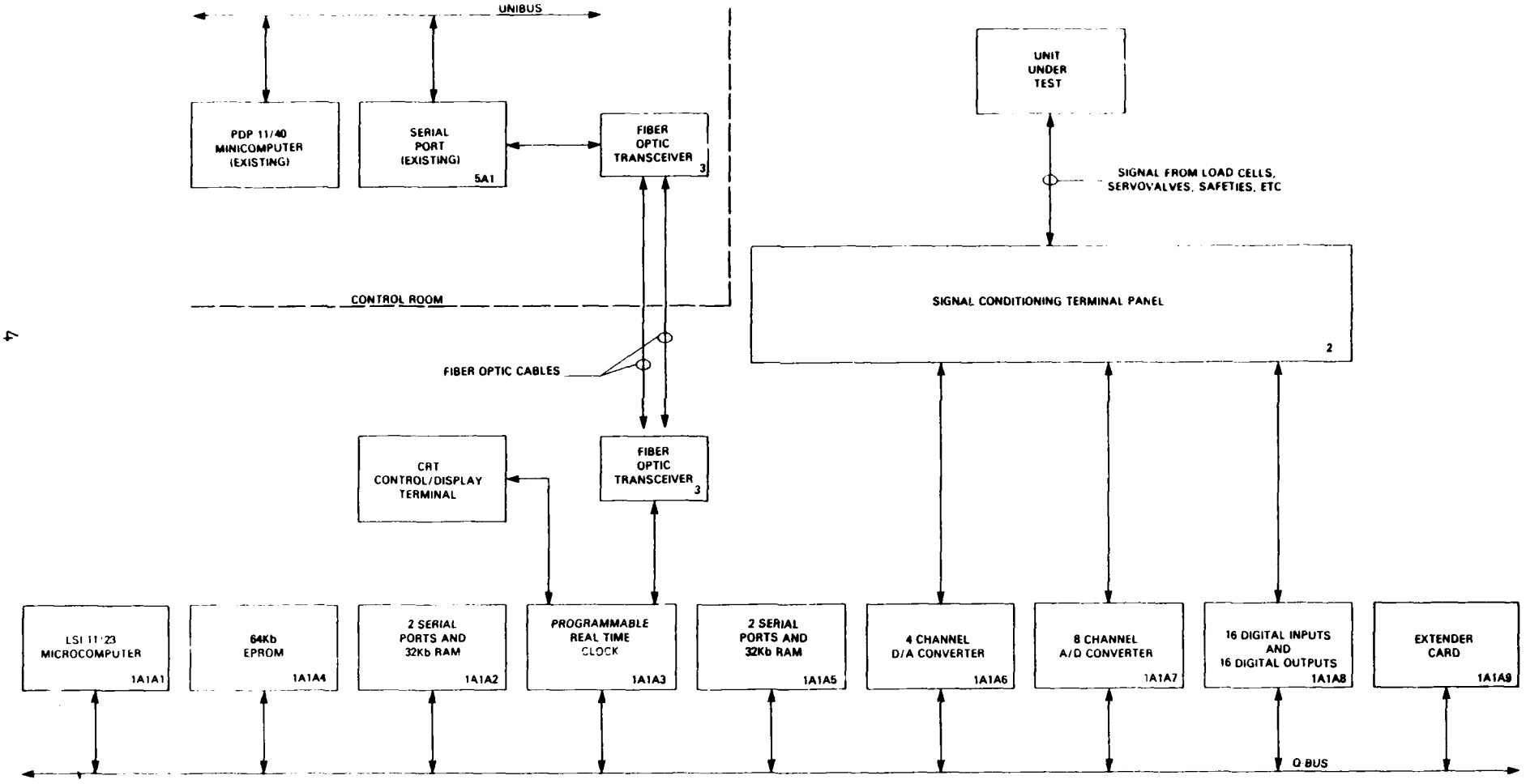


FIGURE 1. DIGITAL SERVOCONTROLLER SYSTEM - SIMPLIFIED BLOCK DIAGRAM

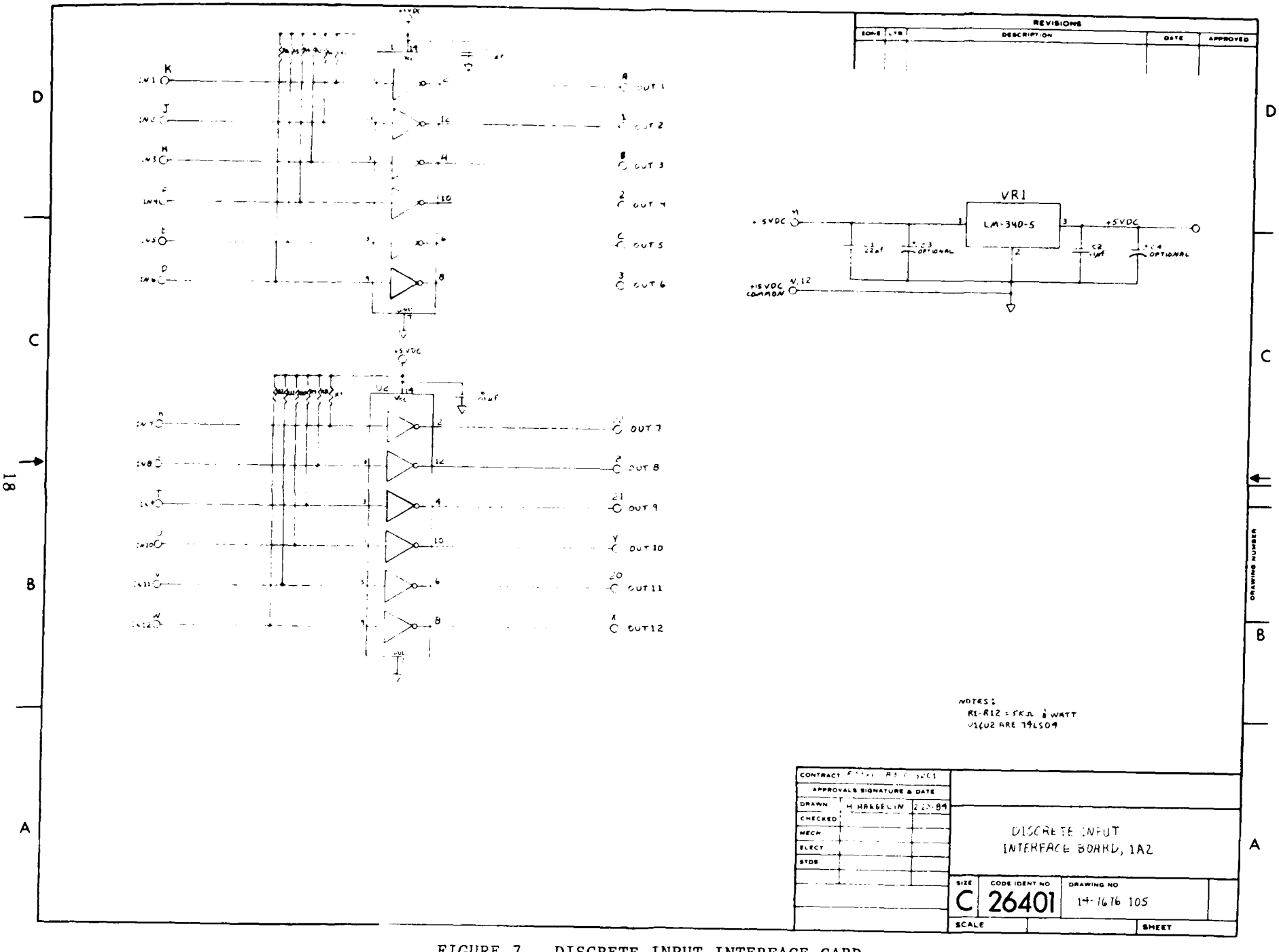


FIGURE 7. DISCRETE INPUT INTERFACE CARD, 1A2 SCHEMATIC DIAGRAM

7.0 INTERFACE CARDS

7.1 Discrete Interface Card, 1A2

The front panel switches: CHANNEL SELECT (1S1), COARSE/FINE SELECT (1S2), and A RAISE/LOWER (1S3) and B RAISE/LOWER (1S4) interface with the microcomputer system through the Discrete Interface Card. The card is located below the Master Console (1A1) as shown on Figure 5. A schematic of the card is given in Figure 7. The inputs to the card are simply routed through inverting buffers to the outputs. A selected switch shorts its respective card input to common. The normal state of the inputs to the card is a TTL high level. Therefore the normal state of the outputs from the card is a TTL low level. Twelve inputs are allowed for this card. The wiring diagram for the Discrete Interface Card is given in Figure 8. The input assignment for the cards is as follows:

Input 1	SELECT	CHANNEL 1
Input 2	SELECT	CHANNEL 2
Input 3	SELECT	CHANNEL 3
Input 4	SELECT	CHANNEL 4
Input 5	RAISE	A
Input 6	LOWER	A
Input 7	RAISE	B
Input 8	LOWER	B
Input 9	SELECT	
Input 10	SPARE	COARSE/FINE (C = "1" F = "0")
Input 11	SPARE	
Input 12	SPARE	

7.2 Servo Driver Card, 2A5 through 2A8

For each control loop, the output signal of the servocontroller system is used to drive its respective servovalve. The nature of the servovalve requires that the bipolar ±10 VDC output from the D/A converter be converted into a proportional current. This is the function of the Servo Driver Card. Figure 9 shows the schematic along with resistor values needed to achieve different current outputs. An AD308 operational amplifier is configured in a non-inverting voltage-to-current mode. The input is attenuated by two to keep the amplifier from saturating at the high end. It is expected that the servovalve be "floating" (not grounded) when connected to the driver. Figure 10 gives the wiring for each Servo Driver Card. These cards are housed in the card cage located on the Signal Conditioning Terminal Panel as shown in Figure 4. See Appendix A for specifications on the AD308.

7.3 Strain Gauge Signal Conditioning Cards, 2A1-2A4

Feedback to the servocontroller system is provided by load cells located on the unit under test. These signals are typically low level (millivolt) in amplitude. An Analog Devices strain gauge transducer is used to amplify this low-level signal to a high-level signal (±10 VDC). The transducer is a Model 2B31K and incorporates the following features:

- 16 diode-clamped data input lines
- 16 latched output lines
- Four control lines
- Logic compatible with TTL or DTL devices
- Data transfer rate of 40 K words per second

Specifications

• Identification	M7941
• Size	Double
• Dimensions	5.25 in. × 8.5 in.
• Power Requirements	+5 VDC ±5%, 0.9A
• Bus Loads	ac 1.4 unit loads, dc 1 unit load

The DRV11 occupies Slot Number 12 in the microcomputer system card cage. See Microcomputers Interfaces Handbook, Digital Equipment Corp., 1982.

6.9 Extender Card, 1A1A9

An extender card will be provided to facilitate system trouble-shooting and maintenance. The extender card will be stored in Slot Number 6 in the microcomputer system.

This MRV11-C occupies Slot Number 5 in the microcomputer system card cage. See Microcomputers Interfaces Handbook, Digital Equipment Corp., 1982.

6.6 Analog to Digital Converter Module, 1A1A7

Feedback signals from strain gage signal conditioning cards are input to a Data Translation, Inc., DT2764 A/D converter. The DT2764 has low level range analog input capability, allowing full scale input ranges of ±10 VDC. The DT2764 contains the following features:

- 8-channel differential inputs
- 12-bit resolution
- 31 kHz throughput at 10 V input range
- 100 megohm input impedance
- ±15 VDC max input

Specifications

• Size	Double
• Dimensions	5.25 in. × 8.5 in.
• Power requirements	+5 VDC ±5%, 1.5A

The DT2764 occupies Slot Number 11 in the microcomputer system card cage. See User Manual for DT2762 Series, Data Translation, Inc., 1979.

6.7 Digital to Analog Converter Module, 1A1A6

Command signals to the servovalves controlling the hydraulic jacks will come from an AAV11-C D/A converter. The D/A will convert a 12-bit word, provided by the control computer, and generate a -10 V to +10 VDC output signal which is proportional to the input. The AAV11-C contains the following features:

- 4-channel analog outputs
- User-selectable output ranges 0 to +10 V and -10 V to +10 V at 20 mA
- 12-bit resolution
- Four TTL compatible digital outputs

Specifications

• Identification	A6006
• Size	Double
• Dimensions	5.25 in. × 8.5 in.
• Power requirements	+5 VDC ±5%, 1.5A

The AAV11-C occupies Slot Number 10 in the microcomputer system card cage. See Microcomputers Interfaces Handbook, Digital Equipment Corp., 1982.

6.8 Parallel Line Interface Module, 1A1A8

The control computer will utilize a DRV11 parallel line unit to monitor the status of the front panel switches. System status outputs are made available for interfacing. The DRV11 contains the following features:

The KWV11-C occupies Slot Number 3 in the microcomputer system card cage. See Microcomputers Interface Handbook, Digital Equipment Corp., 1982.

6.4 Memory and Asynchronous Serial Line Interface, 1A1A2, 1A1A5

Two MXV11-AC's will be utilized each providing 32 Kbytes of random access memory (RAM) and two asynchronous serial line interfaces for the control computer. The RAM will contain the load table values and other program variables required by the computer. Serial Line 1 will be used by the CRT control/display terminal and Serial Line 0 will be used by the master unit. The MXV11-AC contains the following features:

- 32 Kbytes of memory with dynamic refresh
- Optional PROM or system device bootstrap
- Two serial lines
- Crystal clock - 60 Hz

Specifications

• Identification	M8047
• Size	Double
• Dimensions	5.25 in. × 8.5 in.
• Power requirements	+5 VDC ±5%, 1.2A/+12 VDC ±5%, 0.1A
• Bus loads	AC 2 unit loads, DC 2 unit loads

The MXV11-AC's occupy Slots Number 2 and 8 in the microcomputer system card cage. See Microcomputers Interfaces Handbook, Digital Equipment Corp., 1982.

6.5 Erasable Programmable Read Only Memory Module, 1A1A4

A maximum of 64 Kbytes of erasable programmable read only memory (EPROM) will be available for use by the control computer. This will include the system program which will be installed in 4 K × 8-bit 2732 EPROMs and mounted on one MRV11-C memory module. The MRV11-C contains sockets for installation of up to 16 memory chips on one dual-height multilayer module (M8048). The MRV11-C contains the following features:

- 16 K, 32 K or 64 Kbytes of memory
- Choice of EPROM, fusible link PROM or masked ROM
- 18-bit addressing
- Window-mapping capability
- Bootstrap capability

Specifications

• Identification	M8048
• Size	Double
• Dimensions	5.25 in. × 8.5 in.
• Power requirements	+5 VDC ±5%, 0.8A
• Bus loads	AC 2.0 unit loads, DC 1 unit load

- Over 400 possible instructions
- 16-bit word or 8-bit byte addressing
- Eight internal registers
- Stack processing capability
- Asynchronous bus operation
- DMA operation capability
- Power fail and automatic restart hardware
- ODT console emulator

Specifications

• Identification	M8186
• Size	Double
• Dimensions	5.25 in. × 8.5 in.
• Power requirements	+5 VDC ±5%, 2.0A/+12 VDC ±5%, 0.2A
• Bus loads	AC 2 unit loads, DC 1 unit load

The KDF11-AA occupies Slot Number 1 in the microcomputer system. See Microcomputers and Memories, Digital Equipment Corp., 1982.

6.3 Programmable Real Time Clock Module, 1A1A3

The control computer will utilize a KWV11-C programmable real time clock to determine time intervals or count events and generate interrupts to the LSI-11/23 processor at predetermined intervals. A 1 msec clock will be used to synchronize the system. The clock counter has 16 bits of resolution and can be clocked from any of five internal crystal controlled frequencies (100 Hz, 1 kHz, 10 kHz, 100 kHz or 1 MHz), from the line time clock bus line, or from the firing of a Schmitt trigger by an external event. The KWV11-C contains the following features:

- 16-bit presetable counter
- Eight software selectable time bases
- Four operating modes
- Two Schmitt trigger inputs with level adjustment
- Counter/timer overflow output

Specifications

• Identification	M4002
• Size	Double
• Dimensions	5.25 in. × 8.5 in.
• Power requirements	+5 VDC ±5%, 1.0A/+12 VDC ±5%, 50 mA

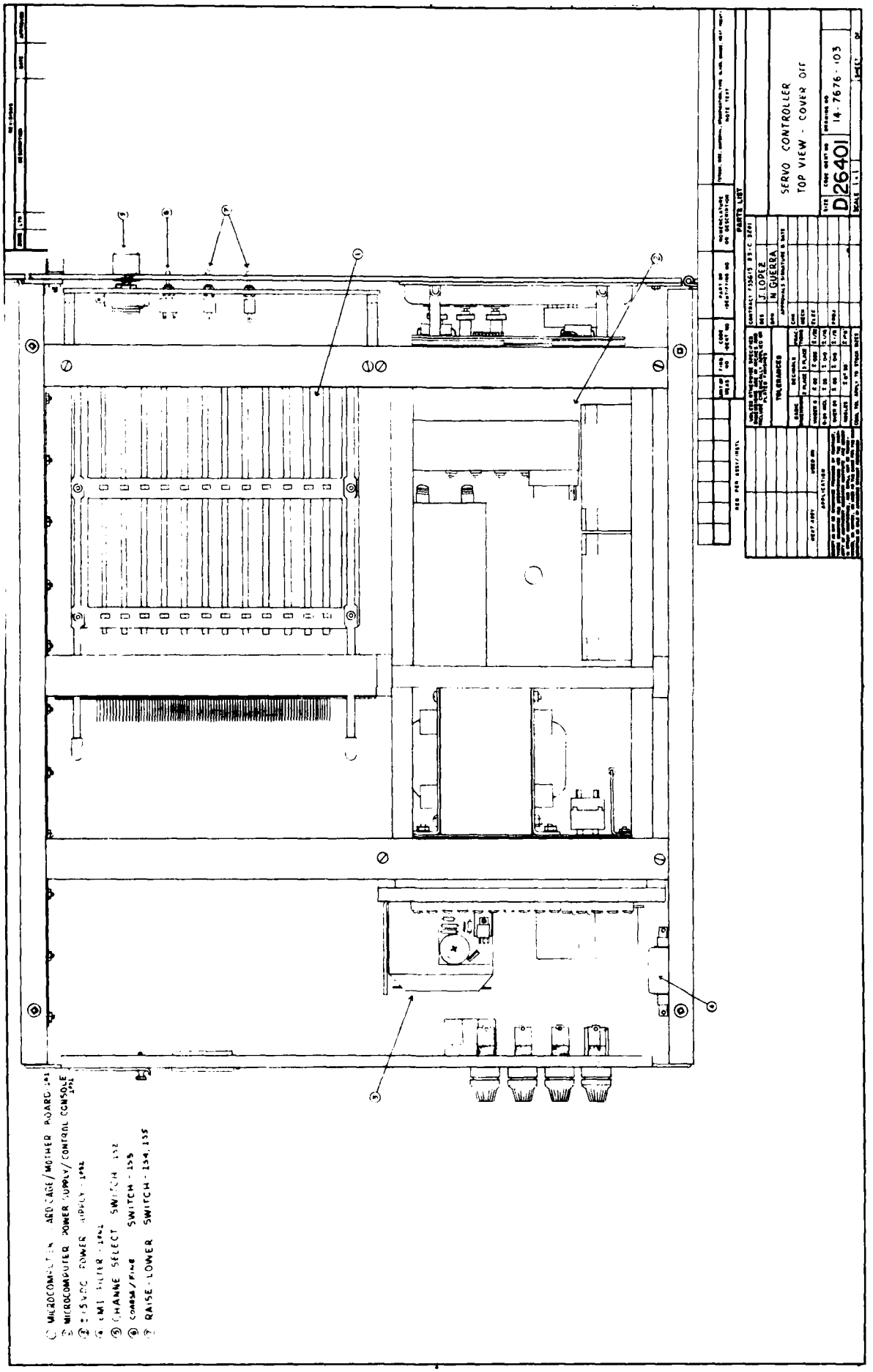
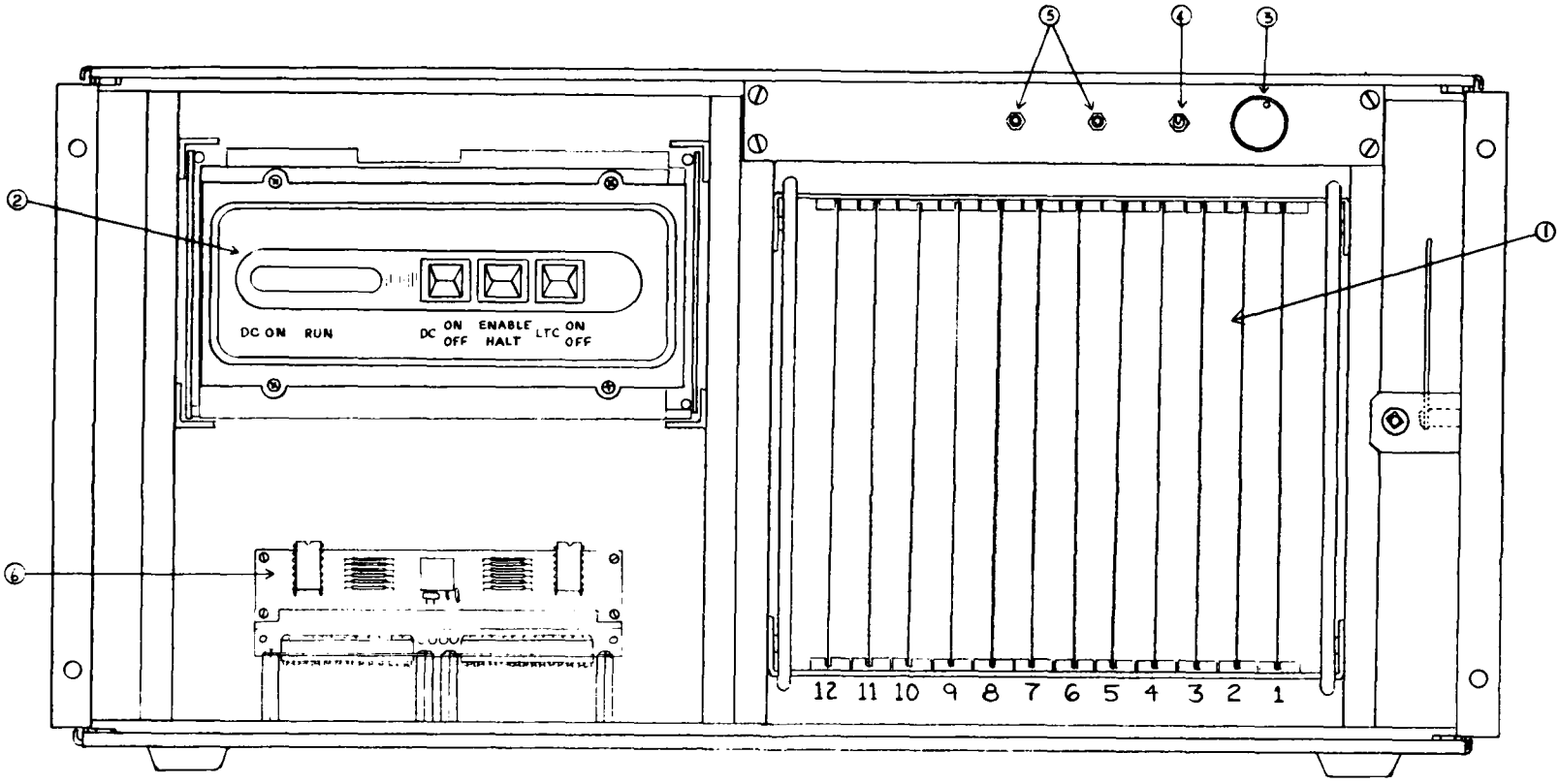


FIGURE 6. SERVOCONTROLLER - TOP VIEW



① MICROCOMPUTER CARD CAGE / MOTHER BOARD - 1A1
② MICROCOMPUTER POWER SUPPLY / CONTROL CONSOLE - 1PS1
③ CHANNEL SELECT SWITCH - 1S2
④ COARSE/FINE SWITCH - 1S3
⑤ RAISE - LOWER SWITCH - 1S4, 1S5
⑥ SERVO CONTROLLER SWITCH INTERFACE CARD - 1A2

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

CONTRACT F33615 83 C 5201		
APPROVALS SIGNATURE & DATE		
DRAWN	N GUERRA	
CHECKED		
MECH		
ELECT		
STDS		
REVISED	H HAEGELIN	3-5-84

SERVO CONTROLLER
FRONT VIEW - PANEL OFF

SIZE	CODE IDENT NO	DRAWING NO
C	26401	14-7676-102

SCALE 1:01 SHEET

FIGURE 5. SERVOCONTROLLER - FRONT VIEW

6.0 MICROCOMPUTER SYSTEM

6.1 Enclosure

The microcomputer system is housed in two components: the master console and card cage. The master console provides the DC power required for the system and generates the proper power up/down signals. The card cage includes the Q-bus backplane into which the system modules connect.

6.1.1 Master Console 1PS1

The master console used to supply the microcomputer system with DC power is a DEC Model H780-H. It is shown in Figures 5 and 6. This console provides the cooling fans required to move air through the microcomputer system. Three switches are found on the front panel of the master console. The DC ON/OFF switch is used to directly switch DC power to the microcomputer system (+5 VDC, ±12 VDC). The ENABLE/HALT switch controls the status of the processor. The LTC ON/OFF switch provides a clock signal used in diagnostics when in the ON position. This switch is normally left in the OFF position. Upon power up/down conditions, the master console automatically sequences the BPOK and BDCOK bus signals for proper operation. Two indicator LEDs are located on the front panel for monitoring the processor status. One is DC ON indicating that DC power is being applied to the system backplane. The other indicator, RUN, indicates whether the processor is in a RUN mode or not. See Microcomputer Interfaces Handbook, Digital Equipment Corp., 1982, for complete details.

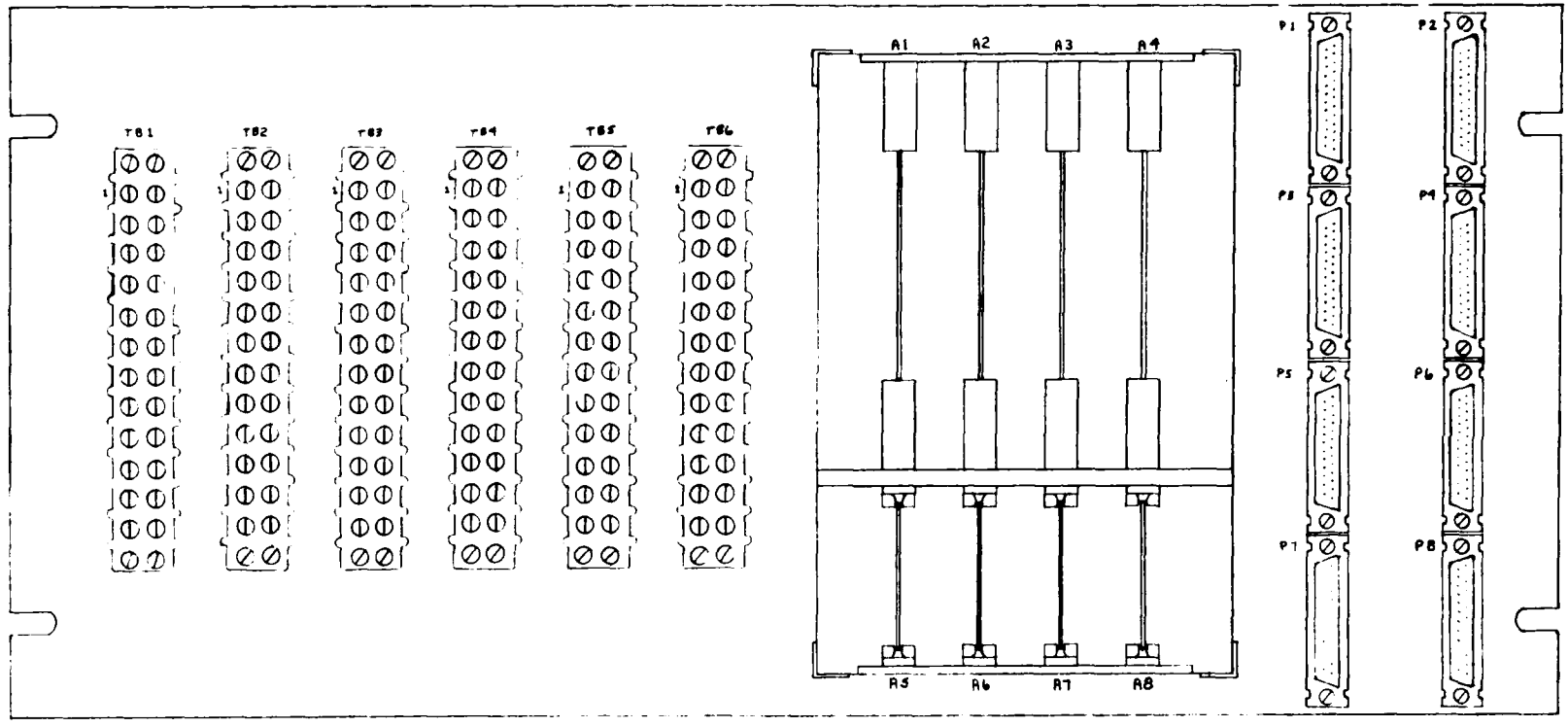
6.1.2 Card Cage, 1A1

The card cage used to house the microcomputer system is a dual wide 12-slot LSI-11 (Q-bus) structured backplane with card guides. This card cage is available from DEC as the H9281-BC. Its location within the servocontroller enclosure is shown in Figure 5. It is designed to accept double-height modules only. The slots are numbered 1 to 12 from right to left in order of decreasing interrupt priority. The microcomputer system modules are installed as illustrated in Figure 5. See Microcomputer Interfaces Handbook, Digital Equipment Corp., 1982, for complete details.

6.2 Processor Module, 1A1A1

The heart of the LSI-11/23 microcomputer system is the KDF11-AA microprocessor module. The KDF11-AA is a 16-bit, high-performance microprocessor contained on one dual-height multilayer module (M8186). The KDF11-AA contains the following features:

- Four-level vectored interrupts
- Optional memory management unit for up to 265 Kbyte addressing capability
- Optional floating point processor
- Memory parity error detection



NOTES: A1-A4 - STRAIN GAGE SIGNAL CONDITIONING CARD
A5-A8 - SERVODRIVER CARDS

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

CONTRACT F33615-83-C-3201		
APPROVALS SIGNATURE & DATE		
DRAWN	H HAGGELIN	2-20-84
CHECKED		
MECH		
ELECT		
STDS		

SIGNAL CONDITIONING
TERMINAL PANEL, 2

SIZE	CODE IDENT NO	DRAWING NO
C	26401	14-7676-104

SCALE | SHEET

DRAWING NUMBER

FIGURE 4. SIGNAL CONDITIONING TERMINAL PANEL, 2

5.0 SIGNAL CONDITIONING TERMINAL PANEL, 2

The interface between the servocontroller system and the hydraulic system is accomplished at this panel. The panel and the components which are mounted on it are shown in Figure 4. Eight D-type Connectors 2P1 through 2P8 are mounted on the panel and are used for direct interface to the microcomputer system. 2P1 interfaces with D/A Module, 1A1A6. 2P2 interfaces with A/D Module, 1A1A5. 2P3 and 2P4 interface with Parallel Line Interface Module, 1A1A7. 2P5 through 2P8 are provided as spare connectors. The built-in card cage houses the Strain Gauge Signal Conditioning Cards 2A1 through 2A4 and Servo Driver Cards 2A5 through 2A8. Wiring between the connectors, interface cards and hydraulic system is made using the terminal blocks provided on the Panel 2TB1 through 2TB6.

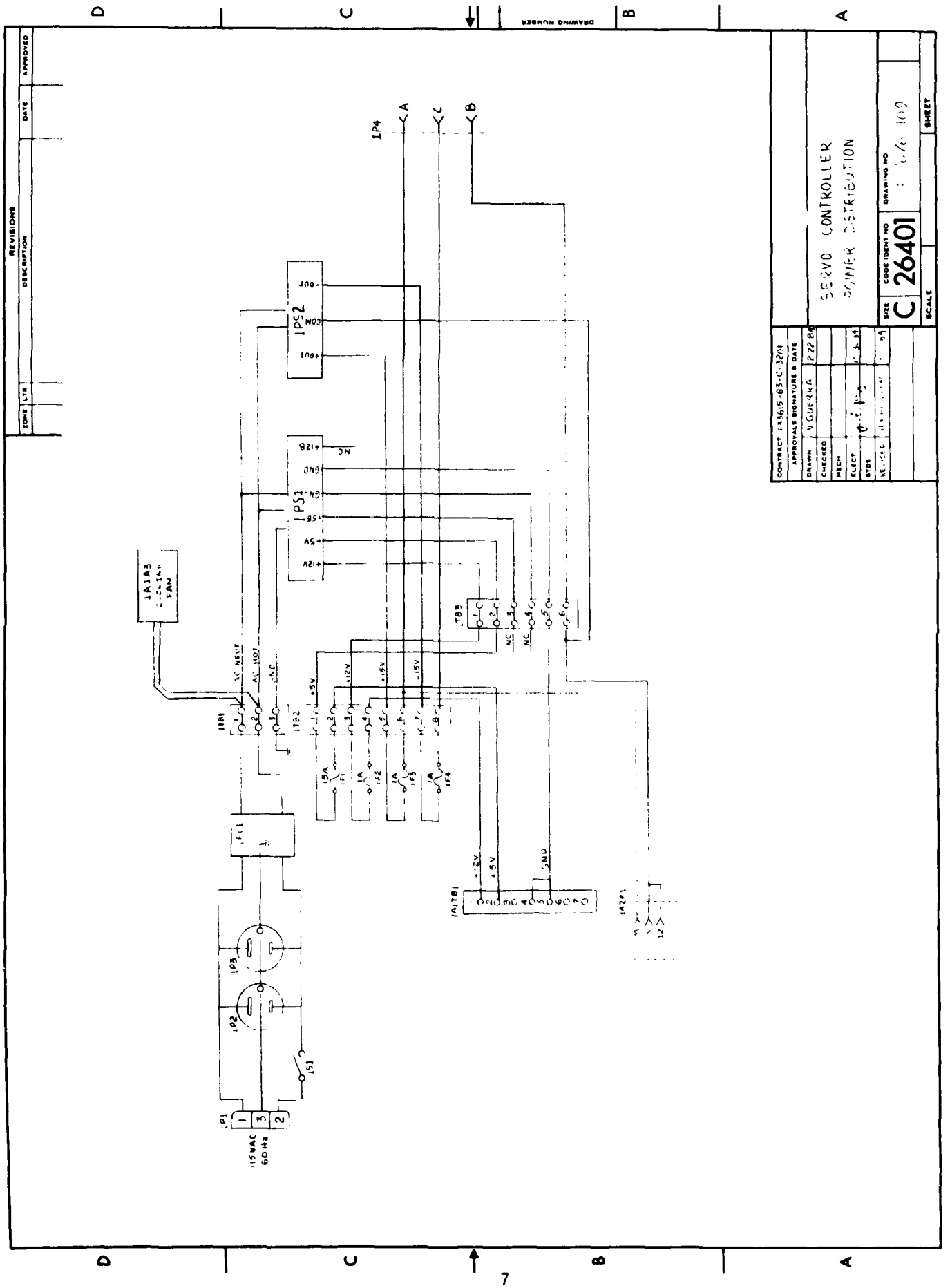


FIGURE 3. SERVOCONTROLLER

4.0 SYSTEM ENCLOSURE, 1

4.1 AC Power

The digital servocontroller system is powered by 120 VAC at 60 Hz. Figure 3 shows the distribution of the AC power within the system. The input power enters the system through the Power Connector 1P1, located on the rear of the enclosure. Power is applied to the system through switch 1S1, which is also located on the rear of the enclosure. Auxiliary power connectors 1P2 and 1P3 are provided at the rear of the enclosure. The input power to the system is filtered through 1FL1 and is used to supply power to the microcomputer system 1PS1 and the auxiliary ±15 VDC Power Supply 1PS2.

4.2 ±15 VDC Power Supply, 1PS2

This small linear power supply provides DC power to the circuits located on the Signal Conditioning Terminal Panel, 2, through Cable W2. These circuits include the Strain Gauge Signal Conditioning Cards 2A1 through 2A4 and the Servo Driver Cards 2A5 through 2A8. Additionally, 1PS2 supplies DC power to the Discrete Interface Card located in the system enclosure. Figure 3 shows the wiring of 1PS1 within the system enclosure.

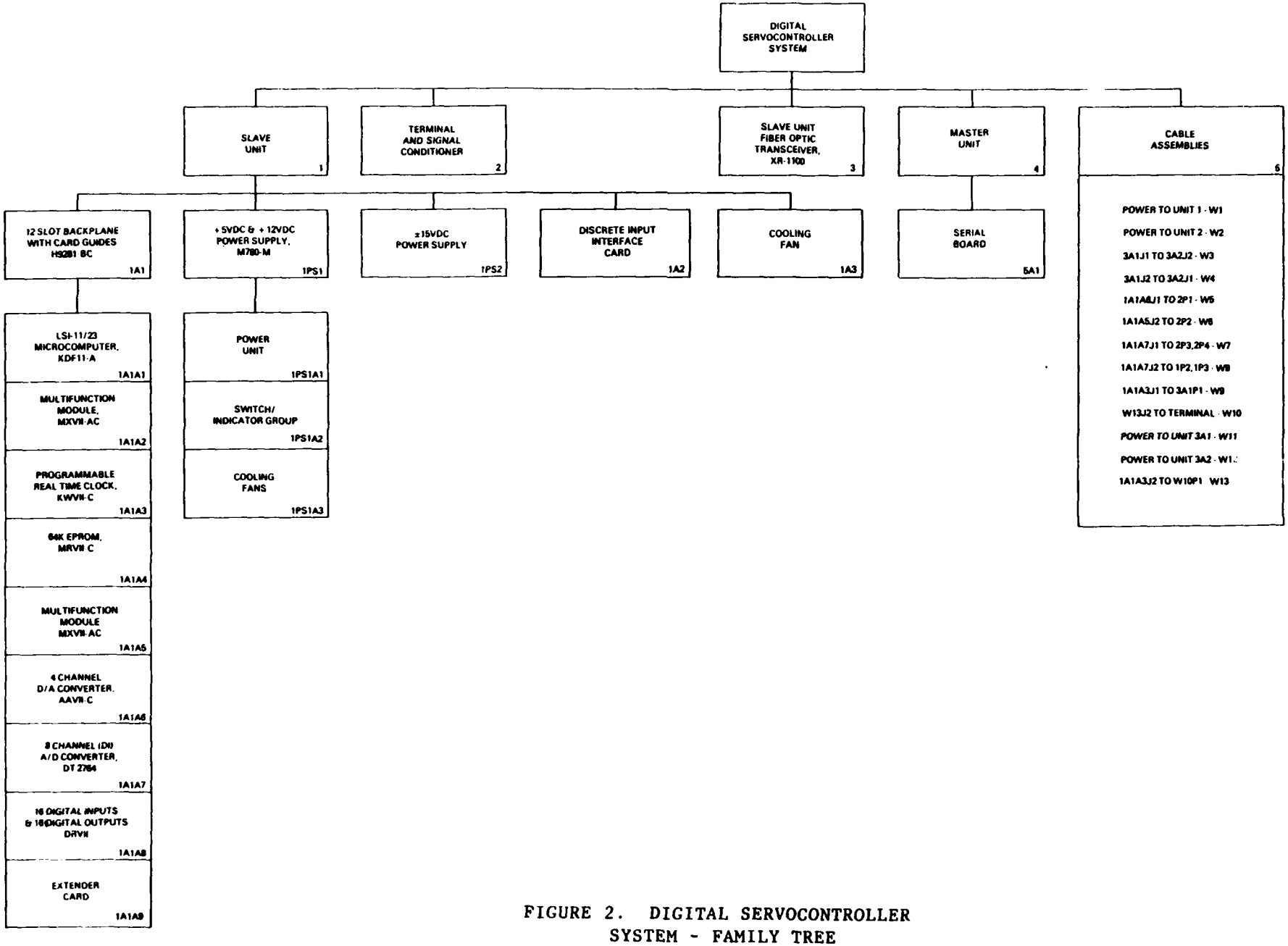


FIGURE 2. DIGITAL SERVOCONTROLLER SYSTEM - FAMILY TREE

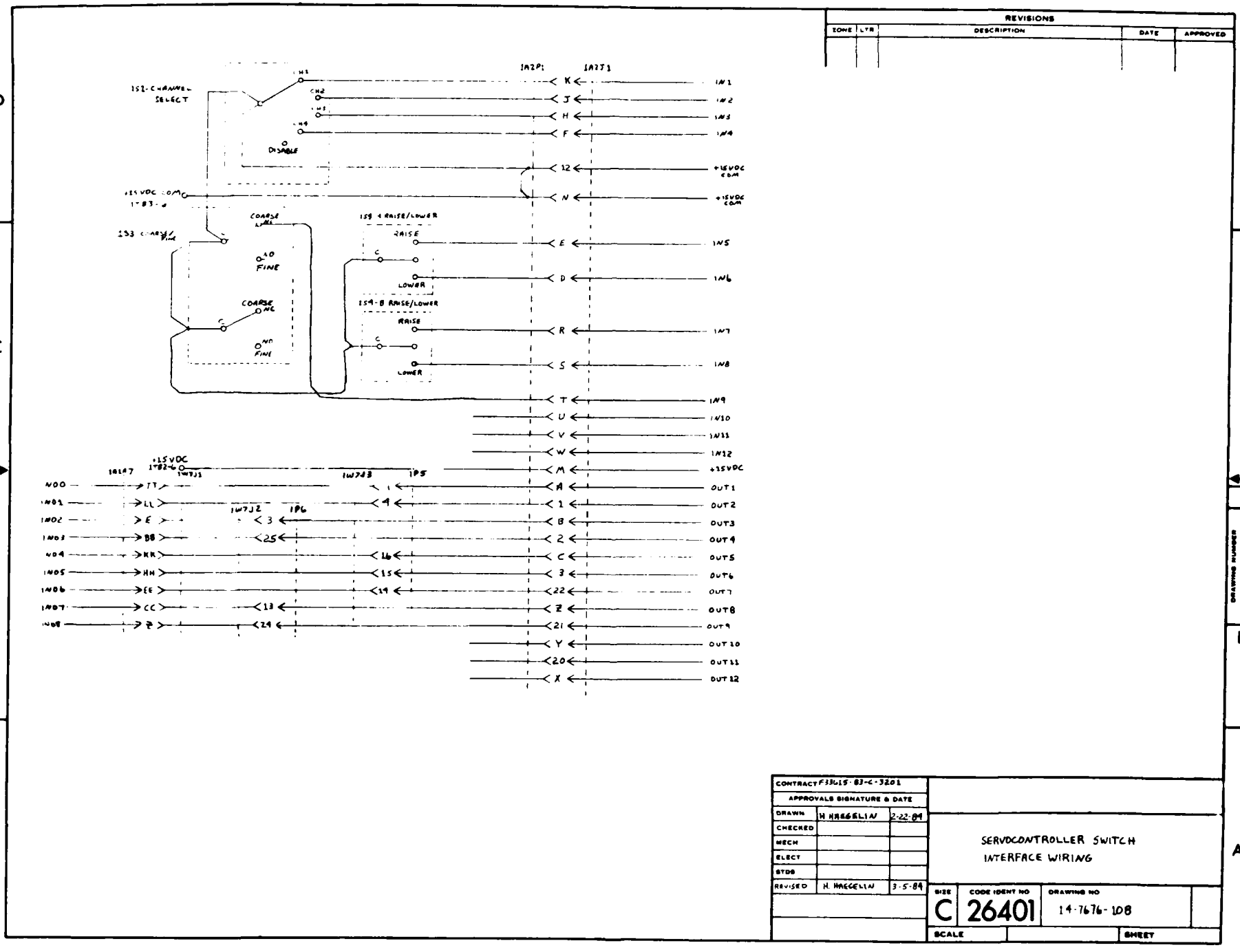


FIGURE 8. DISCRETE INPUT INTERFACE CARD 1A2 WIRING DIAGRAM

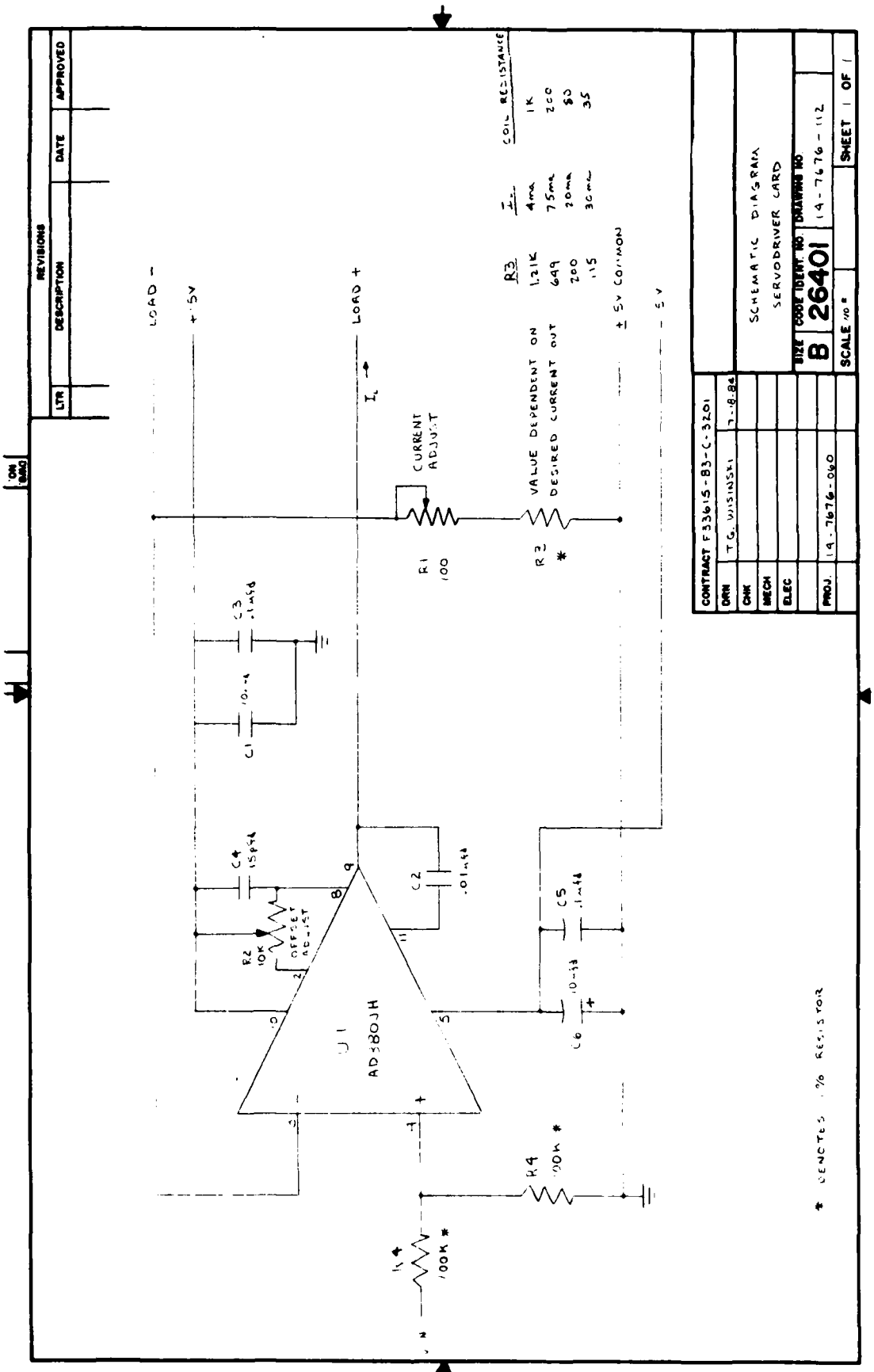


FIGURE 9. SERVO DRIVER CARD, SCHEMATIC DIAGRAM

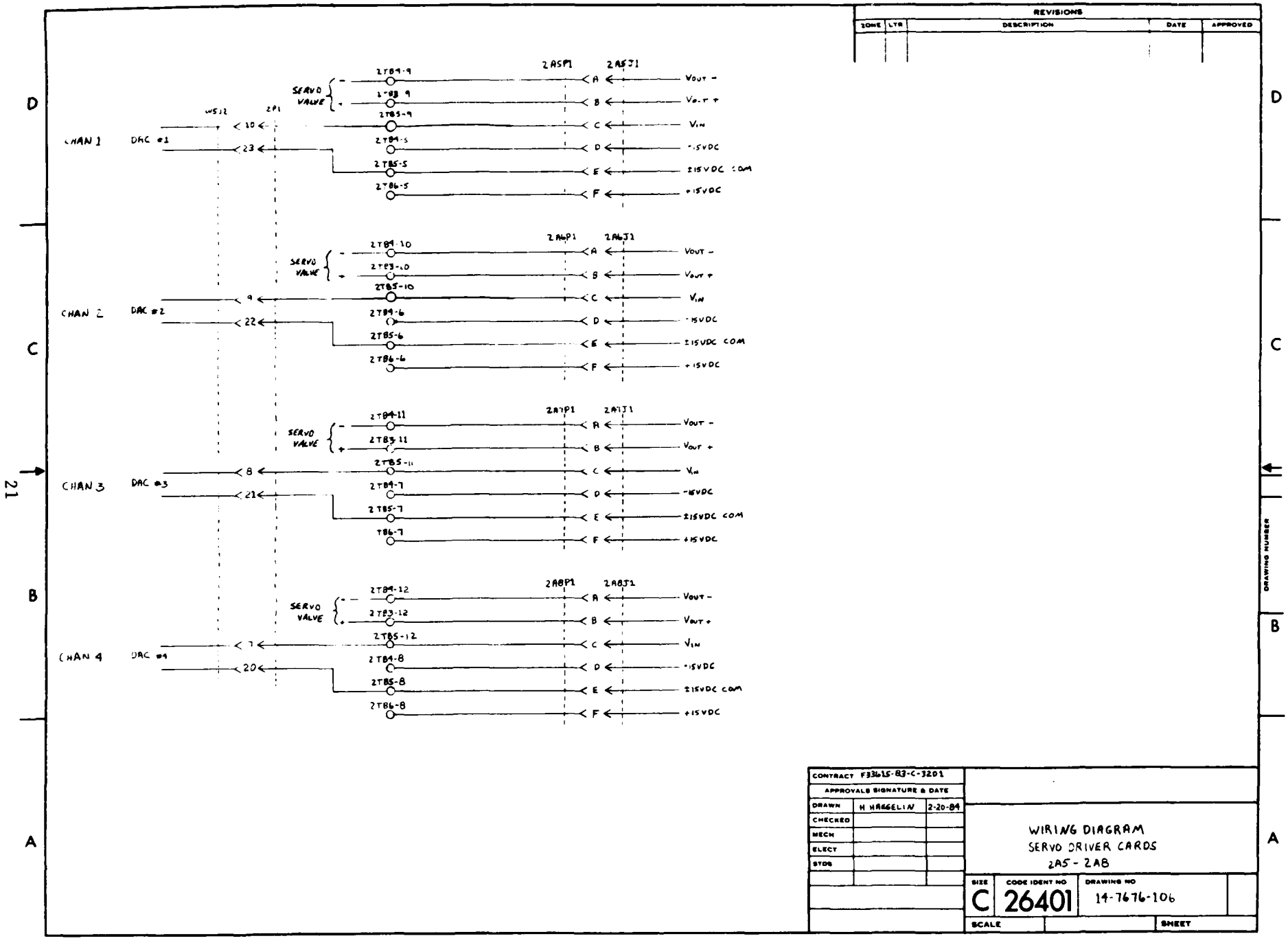


FIGURE 10. SERVO DRIVER CARDS, 2A5-2A8, WIRING DIAGRAM

(1) Programmable gain
(2) Adjustable low-pass filter
(3) Input/output protection
(4) Programmable transducer excitation

In order to ease the interface, the 2B31K has been installed on an AC1213 printed circuit card. This card provides the adjustable potentiometers required to calibrate the signal conditioning circuit. Figures 11 and 12 provide the wiring diagrams for each of these signal conditioning cards. The cards are housed in the card cage on the Signal Conditioning Terminal Panel as shown in Figure 4. See Appendix A for manufacturer specifications of these modules.

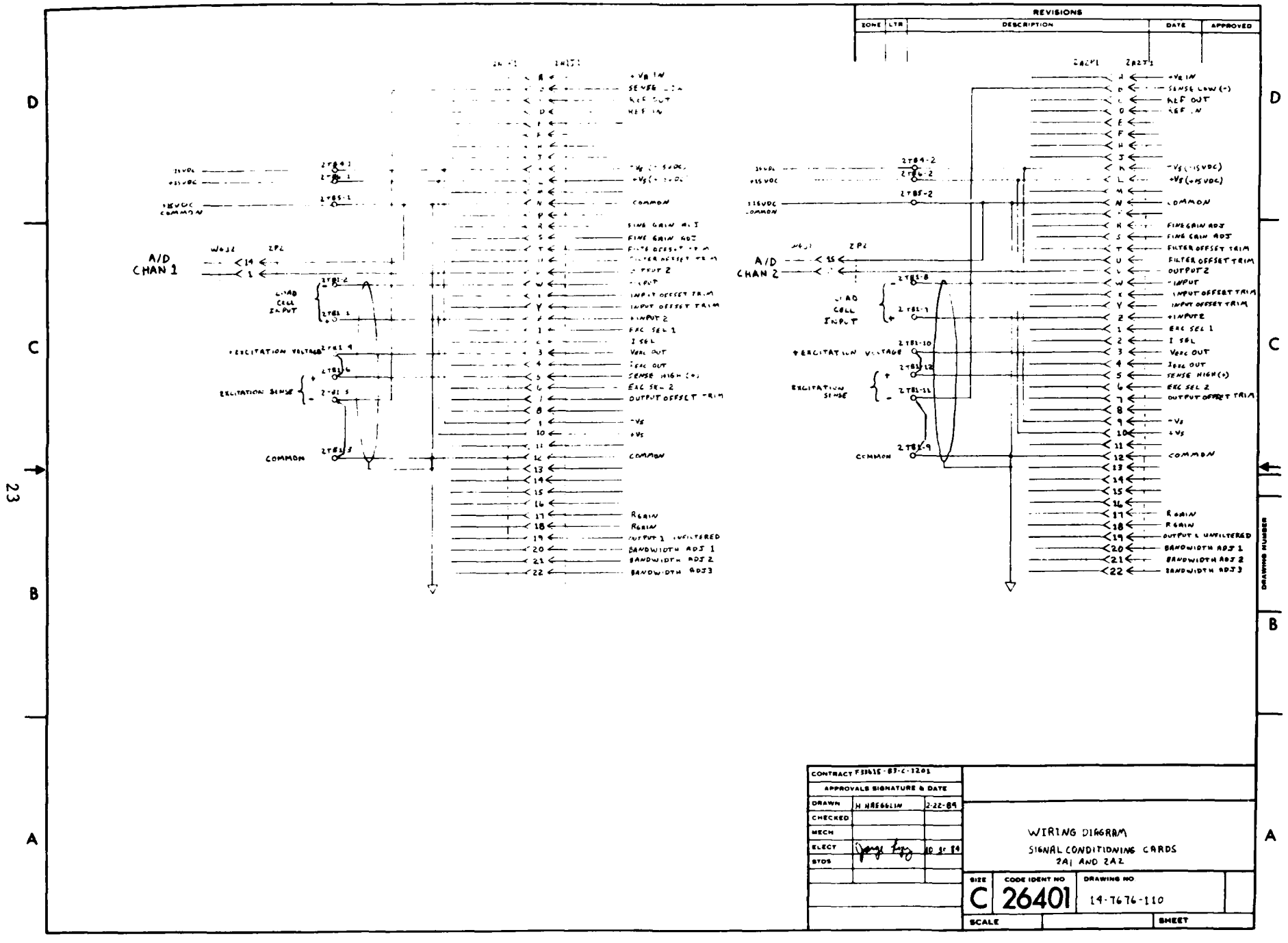


FIGURE 11. STRAIN GAUGE SIGNAL CONDITIONING CARDS, 2A1 and 2A2, WIRING DIAGRAM

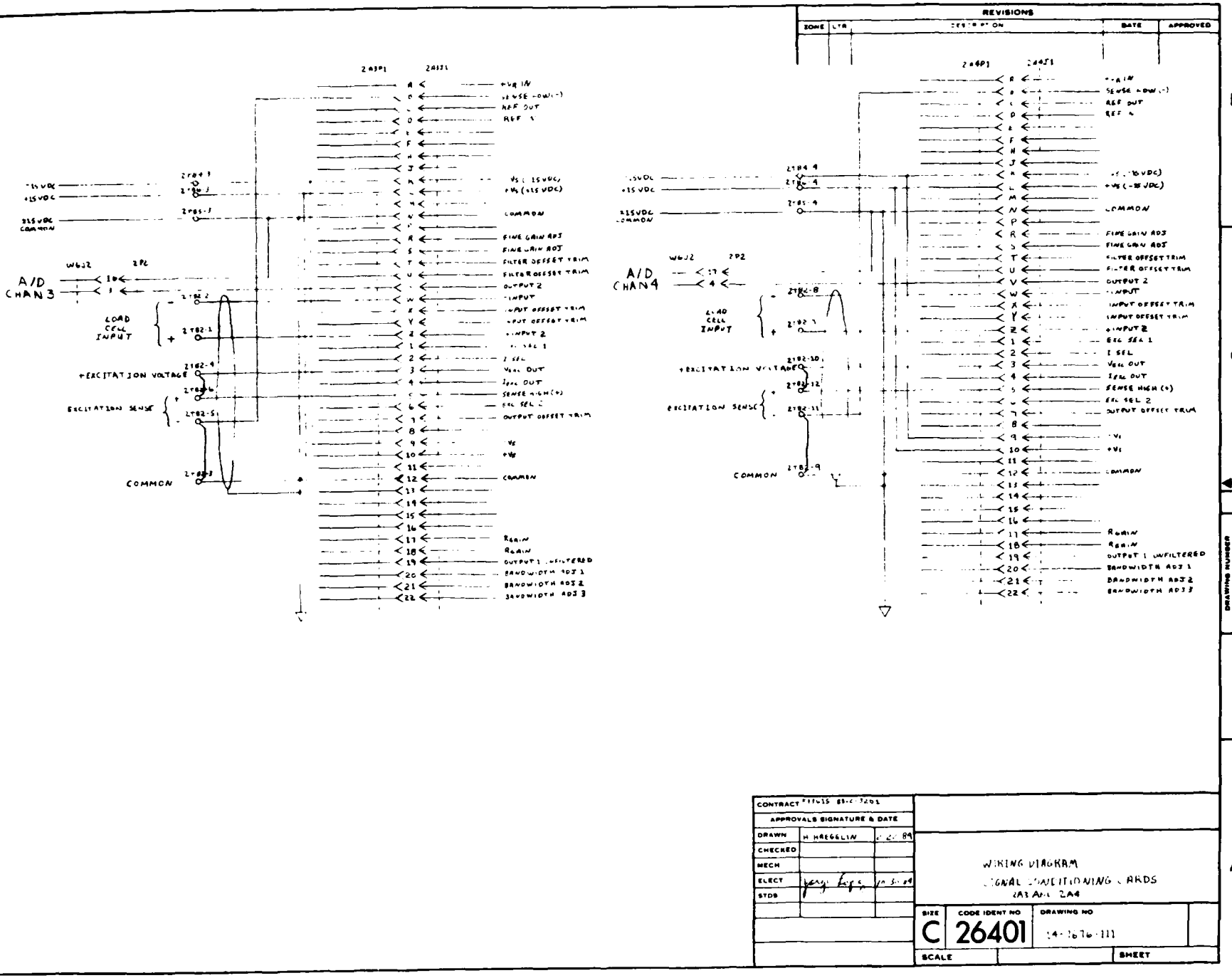


FIGURE 12. STRAIN GAUGE SIGNAL CONDITIONING

8.0 FIBER-OPTIC SYSTEM, 3

The digital servocontroller system has the capability to have profiles downloaded from a master computer. The master computer is located at a remote location relative to the servocontroller system. The link between the two systems is accomplished via a fiber-optic link. A Math Associates, Inc., Fiberlink XR-1150 RS232 Data Transmission System is used for this purpose. The components of the system include two solid state "optical modems" and the fiber-optic cable. The "optical modems" transform the EIA RS232 signals into an optical stream of data operating at an 820 nanometer wavelength. The optical data is transmitted through a 100 micrometer fiber-optic cable. See Appendix A for detailed specifications.

9.0 SYSTEM CABLING

Figure 13 shows the interconnections for the cabling of the servocontroller system. W1 is the power cable. W2 provides the ±15 VDC to the Signal Conditioning Terminal Panel. W3 and W4 are the fiber-optic cables used to link the "master" computer to the servocontroller system. W5 interconnects the D/A module to the Signal Conditioning Terminal Panel. W6 interconnects the A/D module to the Signal Conditioning Terminal Panel. W7 interconnects the Parallel Line Interface Module with the Signal Conditioning Terminal Panel. W8 interconnects the Parallel Line Module with the Discrete Interface Card. W9 is the serial cable interconnecting the servocontroller system to the master computer through the fiber-optic link. W10 is the serial cable interconnecting the servocontroller to the CRT terminal (GFE). W11 and W12 apply DC power to the solid-state modems of the fiber-optic link, 3A1 and 3A2, respectively.

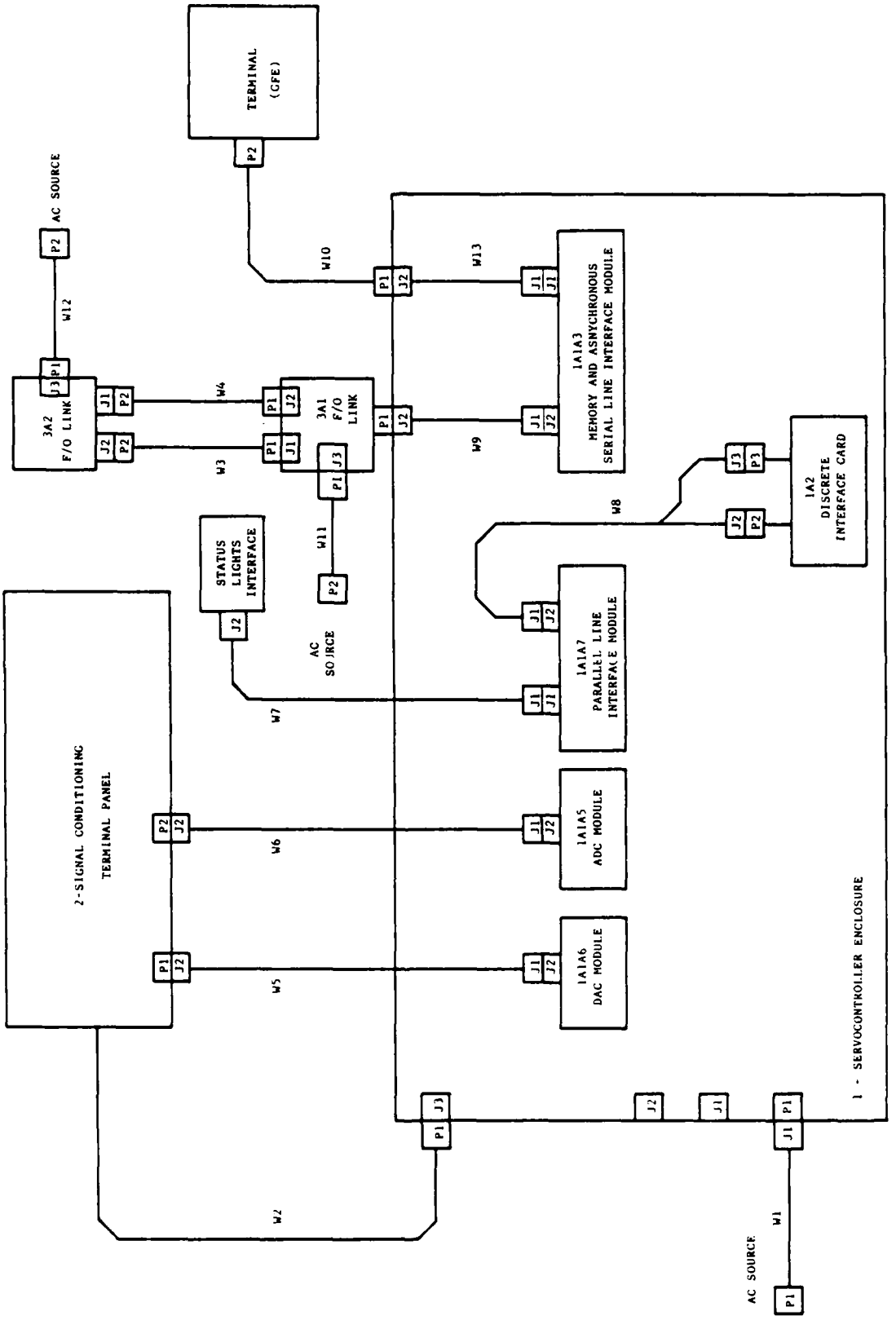


FIGURE 13. SYSTEM CABLING

10.0 CALIBRATION PROCEDURES

10.1 Components to be Calibrated

There are four components within the servocontroller which require calibration. They are:

(1) Digital to Analog Converter Module, 1A1A6
(2) Analog to Digital Converter Module, 1A1A7
(3) Servo Driver Cards, 2A5-2A8
(4) Strain Gauge Signal Conditioning Cards, 2A1-2A4

10.2 Required Equipment

(1) Beckman, Model 3020, Digital Multimeter (DMM) or equivalent
(2) Power Designs, Inc., Model 2010, Precision DC Source or equivalent

10.3 Digital to Analog Converter Module, 1A1A6, Calibration Procedures

(1) Verify that the hydraulics system is shut off.

(2) Verify that power to the servocontroller system is turned off. 1S1 is in the OFF position.

(3) Place the DAC module on the extender card.

(4) Apply power to the servocontroller system. 1S1 is in the ON position.

(5) Initialize the servocontroller system program by moving the DC ON/OFF switch (1PS1) on the front panel to the ON position.

(6) Set the following loop parameters for each channel:

Use the default parameter values except set the LOAD MODE to OPEN for all channels.

(7) Load the following test profile for each channel:

LVL	CMD1 %	CMD2 %	CMD3 %	CMD4 %	CYCLE	SKIP
1	0	0	0	0	1	1
2	0	0	0	0	1	1
3	0	0	0	0	1	1
4	100	100	100	100	1	1
5	100	100	100	100	1	1
6	100	100	100	100	1	1
7	0	0	0	0	1	1

(8) Run the loaded test profile.

For each channel perform the following steps:

(9) Enter the HOLD command when the profile is at a 0 percent command.

(10) Verify that the control output voltage (DAC) is 0 VDC on the terminal display.

(11) Using the DMM, measure the DAC output voltage across:

- Channel 1, DAC A:2TB5-9(+) and 2TB5-5(-)
- Channel 2, DAC B 2TB5-10(+) and 2TB5-6(-)
- Channel 3, DAC C:2TB5-11(+) and 2TB5-7(-)
- Channel 4, DAC D:2TB5-12(+) and 2TB5=8(-)

(12) Adjust the ZERO OFFSET ADJ potentiometer for the corresponding DAC (see Figure 14) to give a 0.001 VDC output reading at the DMM.

(13) Enter the GO command at the terminal to continue the running of the test profile.

(14) Enter the HOLD command at the terminal when the profile reaches a 100 percent command level.

(15) Verify that the control output voltage (DAC) is 10.0 VDC on the terminal display.

(16) Using the DMM, measure the DAC output voltage across:

- Channel 1, DAC A:2TB5-9(+) and 2TB5-5(-)
- Channel 2, DAC B:2TB5-10(+) and 2TB5-6(-)
- Channel 3, DAC C:2TB5-11(+) and 2TB5-7(-)
- Channel 4, DAC D:2TB5-12(+) and 2TB5-8(-)

(17) Adjust the FULL SCALE RANGE ADJ potentiometer for the corresponding DAC (see Figure 14) to give a 9.999 VDC reading on the DMM.

(18) Enter the GO command at the terminal.

(19) Repeat Steps 10 through 19 until no further adjustment is necessary.

(20) Enter the ABORT command at the terminal.

10.4 Analog to Digital Converter Module, 1A1A7, Calibration Procedures

(1) Verify that the hydraulics system is shut off.

(2) Verify that power to the servocontroller system is turned off. 1S1 is in the OFF position.

(3) Place the ADC module on the extender card.

(4) Apply power to the servocontroller system. 1S1 is in the ON position.

(5) Initialize the servocontroller system program by moving the DC ON/OFF switch (1PS1) on the front panel to the ON position.

(6) Remove interface cards 2A1-2A8 from their card cage.

(7) Set the following loop parameters for each channel per Section 10.3.

(8) Load the following test profile for each channel per Section 10.3.

(9) Run the loaded test profile.

(10) Enter the HOLD command at the terminal.

(11) Connect the precision DC source to Pins 1(+) and 14(-) of cable W6J2.

(12) Set the precision DC source to -2.4m VDC.

(13) Adjust the ADC OFFSET ADJ potentiometer (see Figure 15) to give a reading on the FEEDBACK (V) display of between -0.005 VDC and 0.000 VDC.

(14) Set the precision DC source to +9.9927 VDC.

(15) Adjust the ADC RANG ADJ potentiometer (see Figure 15) to give a reading on the FEEDBACK (V) display of between +9.995 and 10.000 VDC.

(16) Repeat Steps 11 through 15 until no further adjustments are required.

(17) Enter the ABORT command at the terminal.

10.5 Servo Driver Cards, 2A5-2A8, Calibration Procedures

(1) Verify tht power to the servocontroller system is off. 1S1 is switched to the OFF position.

(2) Verify that the hydraulic system is shut off.

(3) Remove any external connections between the Signal Conditioning Terminal Panel and the servovalves.

For each Servo Driver Card:

(4) Determine the current required from the card.

(5) Install the appropriately sized resistor R3 on the Servo Driver Card (see Figure 9).

R3 (Ω)	IL	Coil Resistance (Ω)
1.21 K	±4 mA	1 K
649	±7.5 mA	200
200	±20 mA	80
115	±30 mA	35

(6) Install Servo Driver Card into appropriate slot in the card cage.

(7) Place a test load resistor equal to the corresponding coil resistance shown above across:

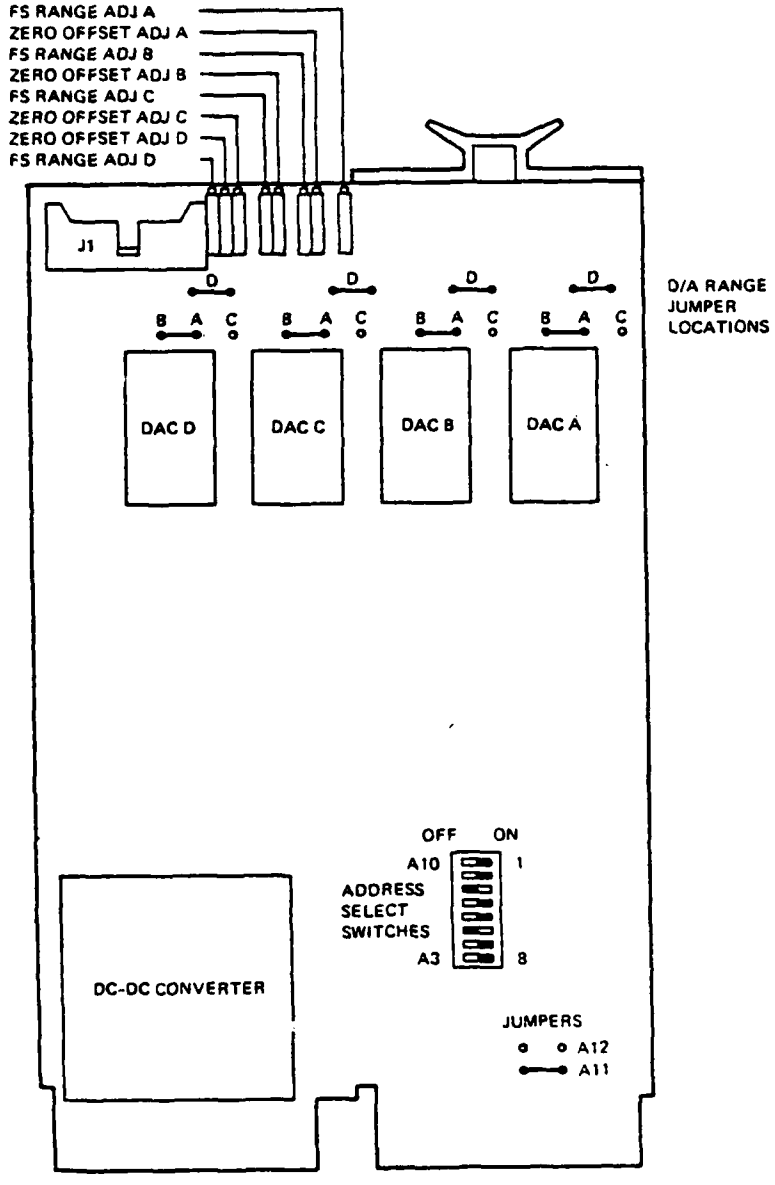


Figure 14. Digital to Analog Converter Module, 1A1A6, Configuration Diagram

- 2A5: (+) 2TB3-9 and (-) 2TB4-9
- 2A6: (+) 2TB3-10 and (-) 2TB4-10
- 2A7: (+) 2TB3-11 and (-) 2TB4-11
- 2A8: (+) 2TB3-12 and (-) 2TB4-12

(8) Place the DMM in line with the test load resistor. The DMM should be set to measure DC current.

(9) Apply power to the servocontroller system. 1S1 switched to the ON position.

(10) Initialize the servocontroller system program by turning the DC ON/OFF switch on the front panel to the ON position.

(11) Set the loop parameters as follows per Section 10.3.

(12) Load the following test profile per Section 10.3.

(13) Initialize the profile run.

(14) Enter the HOLD command on the terminal when the command reaches a 0 percent level.

(15) Verify that the control output voltage is 0.000 VDC.

(16) Adjust the OFFSET ADJUST potentiometer on the Servo Driver Card to read 0.000 mA DC on the DMM.

(17) Enter the GO command on the terminal.

(18) Enter the HOLD command on the terminal when the command reaches a 100 percent level.

(19) Adjust the CURRENT ADJUST potentiometer on the Servo Driver Card to read the required current output.

(20) Enter the ABORT command on the terminal.

(21) Remove the test load resistor.

(22) Power down the servocontroller system. 1S1 switched to OFF position.

(23) Reconnect external cables between the Signal Conditioning Terminal Panel and the servovalves.

10.6 Strain Gauge Signal Conditioning Cards, 2A1-2A4, Calibration Procedures

(1) Verify that the hydraulics system is shut off.

(2) Verify that power to the servocontroller system is turned off. 1S1 is in the OFF position.

DISCOUNT POLICY

For orders of $1,000.00 or more on one Purchase Order, deduct 10%.

For orders of $3,000 or more on one Purchase Order, call for quotation.

Discounts apply to merchandise only.

TERMS

On approved credit: 5% COD, 2/10 — NET 30

1½% per month (18% per annum) charge on accounts unpaid after 30 days.

New accounts — To establish an open account, please provide the name, address and telephone number of your bank and three trade references. Allow 5-7 working days for credit approval.

F.O.B POINT

All shipments are F.O.B. STRONGBOX™ shipping point. Carrier will be of seller's choice unless otherwise specified.

SALES OFFICE HOURS

Our Sales Office is open from 8:00 AM to 3:30 PM (Pacific time) Monday through Thursday, and from 8:00 AM to Noon on Friday. Messages may be left anytime via our telephone answering machine.

WARRANTY

Standard parts may be returned for any reason within 30 days for full credit or refund. Without time limit parts are warranted against defective workmanship and materials.

Prior authorization is required before parts will be accepted for return.

LIABILITY DISCLAIMER

Neither manufacturer nor seller shall be liable for any injury, loss or damage resulting directly or indirectly from the use of or inability to use the product. Before using, user shall determine the suitability of the product for the intended use, and user assumes all risk and liability in connection therewith.

DESIGN CHANGES

STRONGBOX™ reserves the right to change material and design specifications without prior notice.

SPECIAL ORDERS

Dimensions shown in this brochure are STRONGBOX™ standard. Other heights and depths are available. Call or send a print for quotation.

STRONGBOX™

P.O. BOX 84508 L.A., CA 90073 **(213) 204-0472**

STRONGBOX
Parts Specifications
(SB Series)

FRONT PANEL — 0.125" thick, 19.00" wide. 6061-T6 aluminum. EIA notched.

SIDE PANEL — 0.090" thick, 19.00" long. 5052-H32 aluminum. Three rows of holes on ½" centers for mounting panels, card cages, etc.

INTERIOR MOUNTING PANEL — 0.090" thick, 16.37" wide. 5052-H32 aluminum. For use as a rear panel or vertical or horizontal mounting panel.

PERFORATED ALUMINUM COVER — 0.063" thick. 16.85" x 19.12". 3003 aluminum. Assembles with four screws and captive stainless steel nuts.

STRONGBOX™ HANDLE — Standard aluminum handle.

ACCESSORIES

BOTTOM MOUNTING PLATE — 0.090" thick, 16.37" x 18.25". 5052-H32 aluminum. For mounting heavy components. Clear iridite finish.

SOLID BEARING SLIDE— .38" thick. Cad plated steel. Adjustable brackets for assembling to EIA tapped-rail. Extends chassis from 20" to 26".

SOLID ALUMINUM COVER — 0.063" thick, 16.85" x 19.12". 5052-H32 aluminum. Clear anodize finish.

RACK-MOUNT CHASSIS KITS (SB Series)

Each SB series kit contains 1 Front Panel, 2 Side Panels, 1 Interior Mounting Panel, 2 Perforated Aluminum Covers and 2 SB Handles.

.Kits are designated as follows:

Kit Number	Number of Rack Units	Front Panel Height
SB-3	2	3.47"
SB-5	3	5.22"
SB-7	4	6.97"
SB-8	5	8.72"

Order Bottom Mounting Plates, Slides and additional Interior Mounting Panels as separate items.
Add dash "—SAC" to kit number to get Solid instead of perforated covers.

PARTS (SB Series)

Order SB Series parts from the following table. Parts in each column mate.

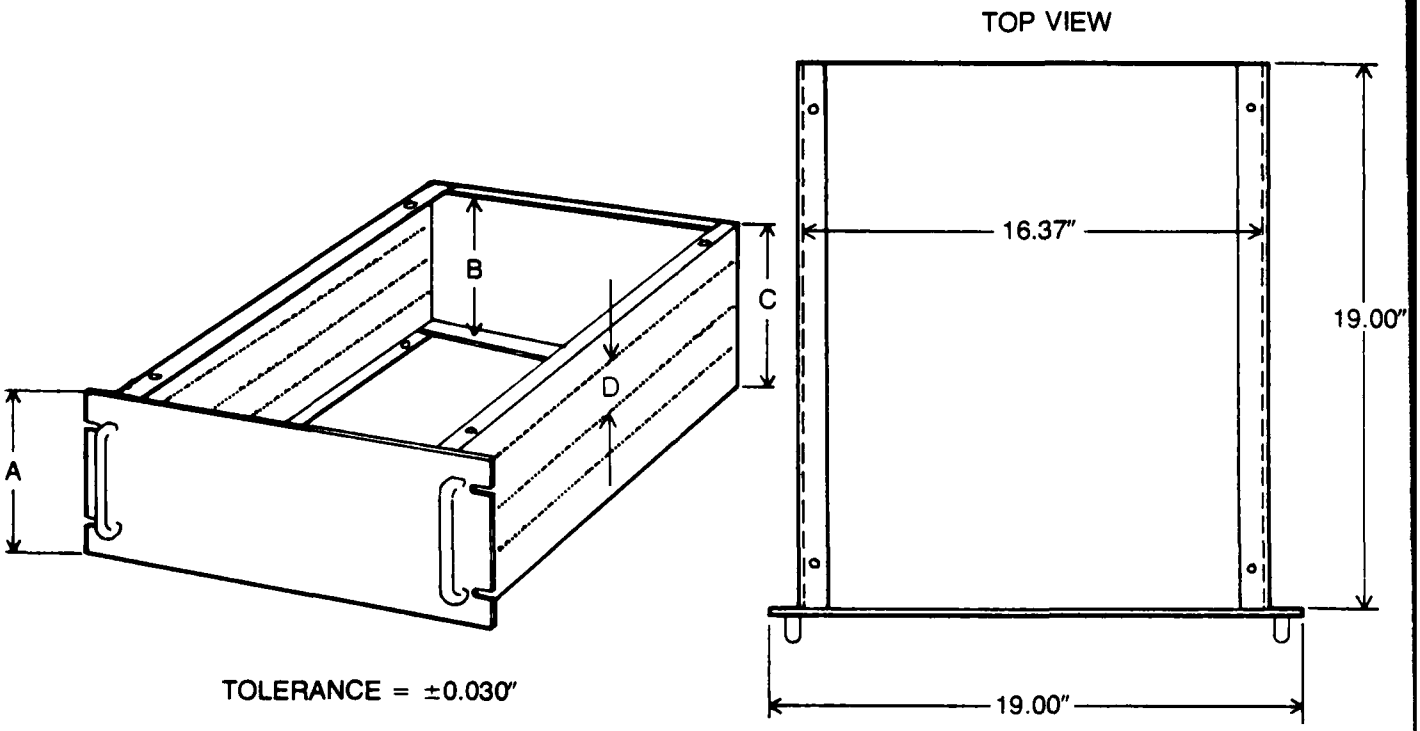
	3"	5"	7"	8"
Front Panel	FP-3	FP-5	FP-7	FP-8
Side Panel	SP-3	SP-5	SP-7	SP-8
Interior Mounting Panel	IMP-3	IMP-5	IMP-7	IMP-8
Perforated Aluminum Cover	PAC	PAC	PAC	PAC
Handle	SBH-3	SBH-5	SBH-7	SBH-8
Bottom Mounting Plate	BMP	BMP	BMP	BMP
Solid Bearing Slide	SLD	SLD	SLD	SLD
Solid Aluminum Cover	SAC	SAC	SAC	SAC

STRONGBOX
Rack-Mount Chassis Units
(SB Series)

SB Series Rack-mount Chassis come standard in four EIA Front Panel heights: 3½", 5¼", 7" and 8¾". (3, 5, 7, 8 nominal.)

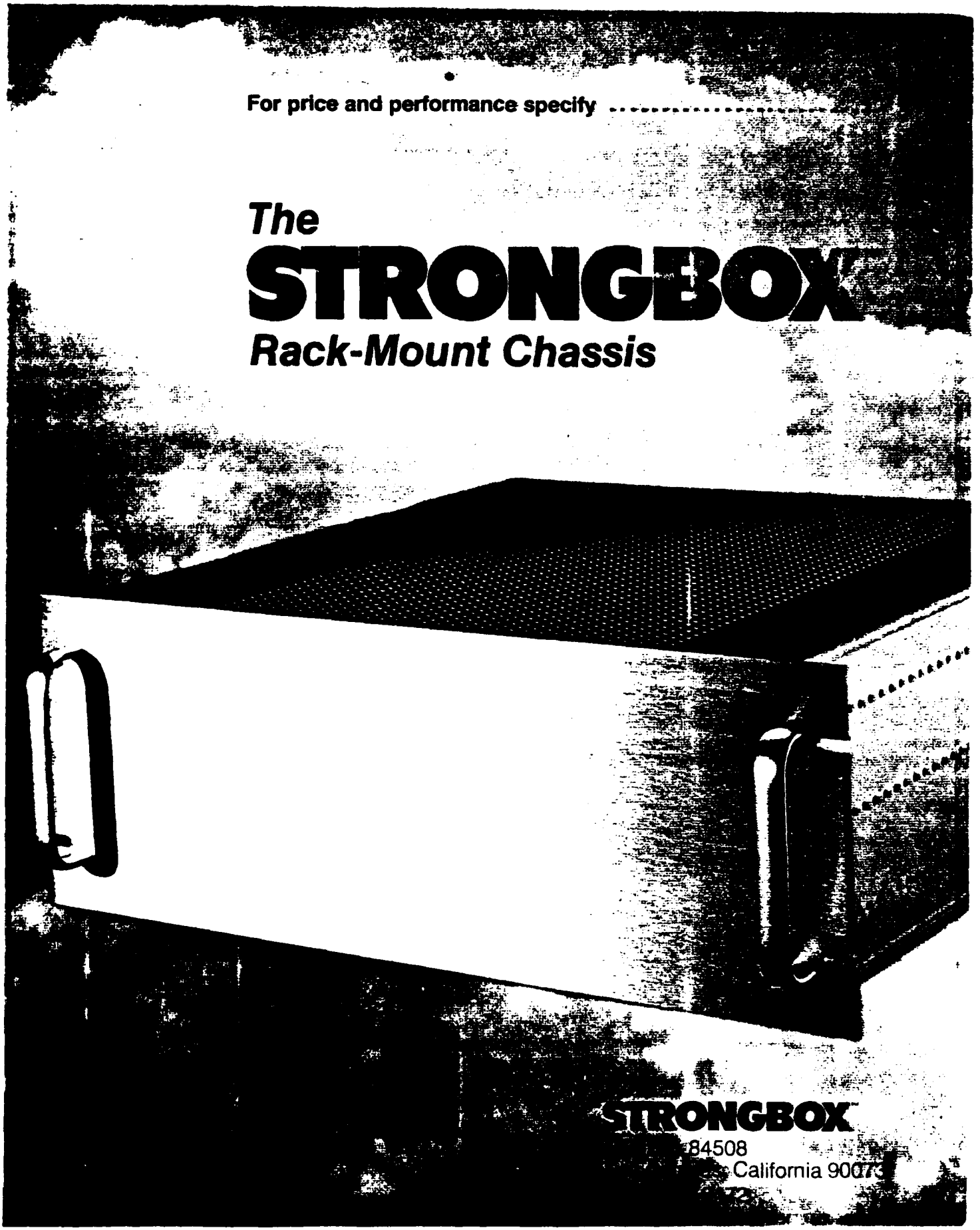
SB Series components can be ordered by the part or in kit form. See parts and kit tables on page 3. Both parts and kits come with all required captive machine hardware. Front, side and mounting panels are clear iridited. Covers and handles are clear anodized. All surfaces are satin grained.

Basic dimensional information is given below. Detailed drawings available on request. Other sizes are available; See Special Orders page 4.



TOLERANCE = ±0.030"

Kit Number	A	B	C	D
SB-3	3.47	3.09	3.15	0.75
SB-5	5.22	4.84	4.90	1.50
SB-7	6.97	6.59	6.65	2.00
SB-8	8.72	8.34	8.40	3.00


For price and performance specify
The
STRONGBOX
Rack-Mount Chassis
STRONGBOX
84508
California 900

APPENDIX A

MANUFACTURER SPECIFICATIONS

APPENDIX A - MANUFACTURER SPECIFICATIONS

11.3 Analog to Digital Converter Module, 1A1A5, Configuration

Configure this module as follows (refer to Figure 15):

Input Range - ±10 VDC
Remove R_g
Remove C_t

11.4 Servo Driver Card, 2A5 to 2A8, Configuration

Configure this module as follows (refer to Figure 9):
Select R3 for required current output from tables below:

R3 (Ω)	I_L (mA)
1.21 K	±4 mA
649	±7.5 mA
200	±20 mA
115	±30 mA

11.5 Strain Gauge Signal Conditioning Card, 2A1 to 2A4, Configuration

Configure this module as follows (refer to Appendix A):

Install the following resistors:

R_G = 274 Ω
R_{SEL1} = 2.15 kΩ
R_{SEL2} = 3.32 kΩ
R_{SEL3} = 649 kΩ

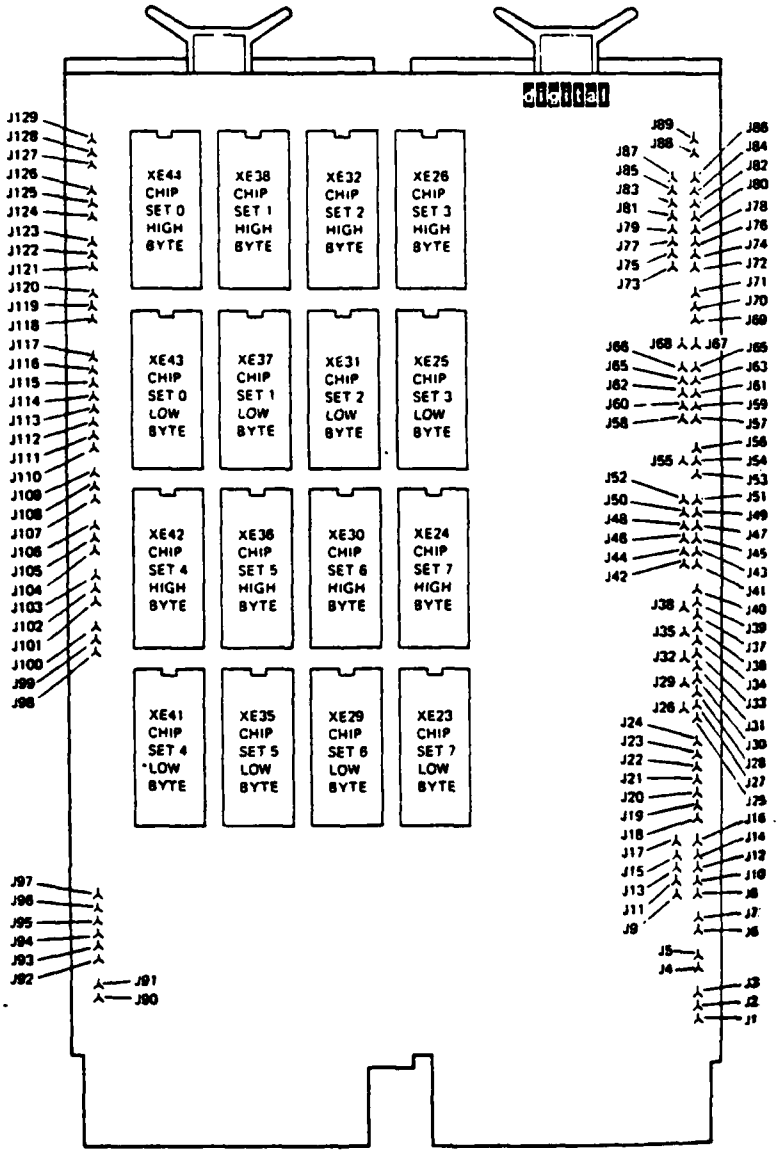


Figure 17. Erasable Programmable Read Only Memory Module, 1A1A4, Jumper Locations

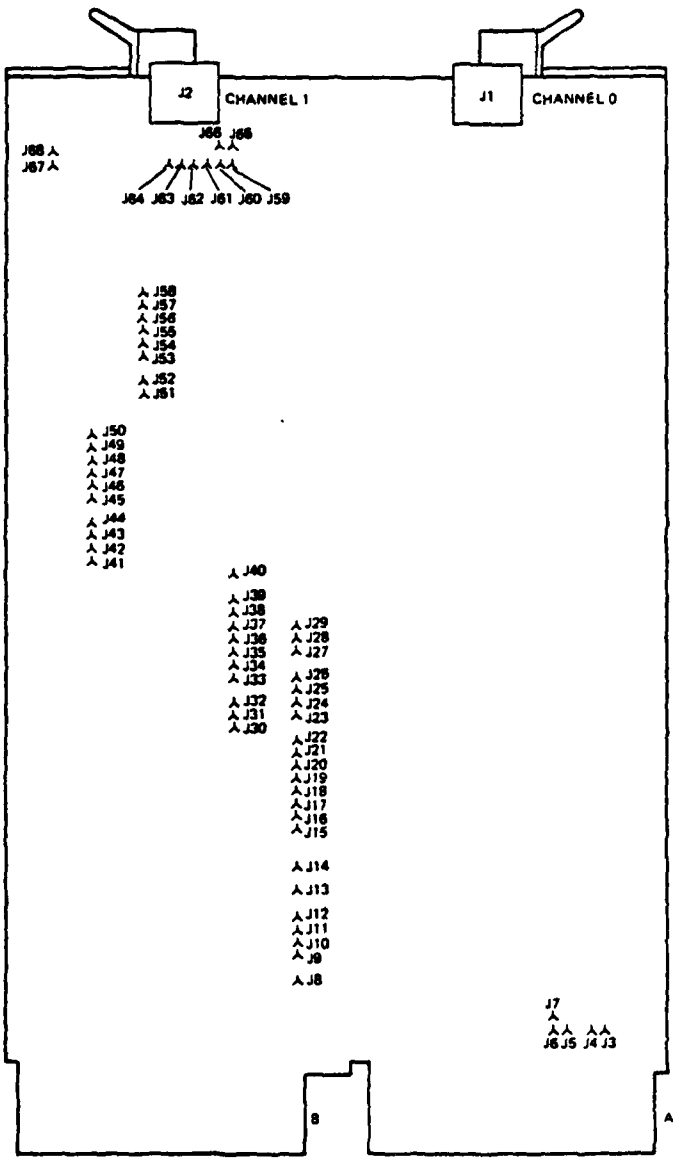


Figure 16. Memory and Asynchronous Serial Line Interface Module, 1A1A2, 1A1A5, Jumper Locations

	Wire Wrap Pins From	To
	J27	J13
	J28	J19
Disable ROM	J21	J8
SLU-0 Baud Rate 9600	J45	J48
SLU-1 Baud Rate 4800	J46	J47

11.2 Erasable Programmable Read Only Memory Module, 1A1A4, Configuration

Configure this module as follows (refer to Figure 17):

	Wire Wrap Pins From	To
CSR Address - 177004_8	J94	J95
Window Enable/Disable	J67	J68
64 KB Window Mode Jumpers		
Low Byte		
CSR Bit 0	J27	J26
1	J30	J29
2	J33	J32
3	J36	J38
4		
High Byte		
CSR Bit 8	J9	J8
9	J11	J10
10	J13	J12
11	J15	J14
12	J17	J16
Enable Low Byte Mux	J69	J71
Address Bit AD11	J112	J113
AD12	J115	J116
Window Starting Address - 160000_8	J51	J52
Disable Bootstrap	J88	J89
ROM Chip Enable	J86	J87
	J84	J85
	J82	J83
	J80	J81
	J78	J79
	J76	J77
	J74	J75
4KX8 EPROM (2732)	J118	J120
	J121	J123
	J124	J126
	J127	J129
	J101	J103
	J98	J100
	J104	J106
	J107	J109
Access Time (250 ns)	J2	J3
DATIO Inhibit	J4	J5

11.0 SYSTEM CONFIGURATION

The following paragraphs in this section describe the configuration on reconfiguration required on the following system components:

(1) Memory and Asynchronous Serial Line Interface Module, 1A1A2 and 1A1A5
(2) Erasable Programmable Read Only Memory Module, 1A1A4
(3) Analog to Digital Converter Module, 1A1A7
(4) Parallel Line Interface Module, 1A1A8
(5) Servo Driver Card, 2A5 to 2A8
(6) Strain Gauge Signal Conditoning Card, 2A1 to 2A4

The remainder of system components should be installed as they are received from the manufacturer, that is factory configured.

11.1 Memory and Asynchronous Serial Line Interface Module, 1A1A2, Configuration

Configure this module as follows (refer to Figure 16)):

1A1A2

RAM Beginning Address - 000000_8 (factory configured)
SLU-0 Address - 176500_8 (factory configured)
SLU-1 Address - 177560_8 (factory configured)
Boot RAM Address - 173000_8 (factory configured)

ROM - 2716	Wire Wrap Pins From	To
	J40	J39
	J38	J36
	J37	J33
	J29	J15
	J21	J22
SLU-0 Baud Rate 9600	J45	J48
SLU-1 Baud Rate 4800	J46	J47
Break Key Disable	Remove jumper J6-J7	

1A1A5

RAM Beginning Address - 100000_8	Wire Wrap Pins From	To
	J30	J33
	J31	J33
	J32	J34
SLU-0 Address - 176510_8	J23	J18
	J24	J12
SLU-1 Address - 176520_8	J26	J16
	J25	J17

(17) Connect the precision DC source to the input of the Strain Gauge Signal Conditioning Card:

2A1, Channel 1: 2TB1-1(+), 2TB1-2(-) to 2TB1-3
2A2, Channel 2: 2TB1-7(+), 2TB1-8(-) to 2TB1-9
2A3, Channel 3: 2TB2-1(+), 2TB2-2(-) to 2TB2-3
2A4, Channel 4: 2TB2-7(+), 2TB2-8(-) to 2TB2-9

(18) Set the output voltage of the precision DC source to the previously calculated full-scale input.

(19) Adjust the FINE SPAN potentiometer on the Strain Gauge Signal Conditioning Card for a reading 9.76 VDC.

(20) Repeat Steps 11 through 20 until no further adjustments are required.

(21) Remove the precision DC source.

(22) Remove previously made jumpers between points on 2TB1 and 2TB2.

(23) Shut down the servocontroller system.

(3) Verify that the proper resistors are in place on each Strain Gauge Signal Conditioning Card (see Section 11).

(4) Apply power to the servocontroller system. 1S1 is in the ON position.

(5) Initialize the servocontroller system program by moving the DC ON/OFF switch (1PS1) on the front panel to the ON position.

For each channel perform the following steps:

Strain Gauge Excitation Voltage Adjustment:

(6) Measure the DC excitation voltage with the DMM across TP1 (+) and TP2 (-) on the Strain Gauge Conditioning Card.

(7) Adjust the EXCITATION ADJ potentiometer on the Strain Gauge Conditioning Card for a 10,000 VDC reading on the DMM.

Offset and full-scale adjustments:

(8) Remove external connectors between the Signal Conditioning Terminal Panel and the servovalves.

(9) Calculate the rated full-scale input from the strain gauges used:

FS (mV) = strain gauge rating (mV/V) x DC excitation (V)

(10) Tie the input to system common as follows:

Channel 1: 2TB1-1 to 2TB1-2 to 2TB1-3 (2A1)
Channel 2: 2TB1-7 to 2TB1-8 to 2TB1-9 (2A2)
Channel 3: 2TB2-1 to 2TB2-2 to 2TB2-3 (2A3)
Channel 4: 2TB2-7 to 2TB2-8 to 2TB2-9 (2A4)

(11) Place the DMM on Pin 3 of the 2B31 module on the Strain Gauge Signal Conditioning Card referenced to TP2.

(12) Adjust the INPUT OFFSET potentiometer on the Strain Gauge Signal Conditioning Card for a 0.000 VDC reading on the DMM.

(13) Place the DMM on TP4 of the Strain Gauge Signal Conditioning Card referenced to TP2.

(14) Adjust the OUTPUT OFFSET potentiometer on the Strain Gauge Signal Conditioning Card for a reading between +10 mVDC and -10 mVDC.

(15) Place the DMM on TP3 of the Strain Gauge Signal Conditioning Card referenced to TP2.

(16) Adjust the FILTER OFFSET potentiometer on the Strain Gauge Signal Conditioning Card for a reading between +1 mVDC and -1 mVDC.

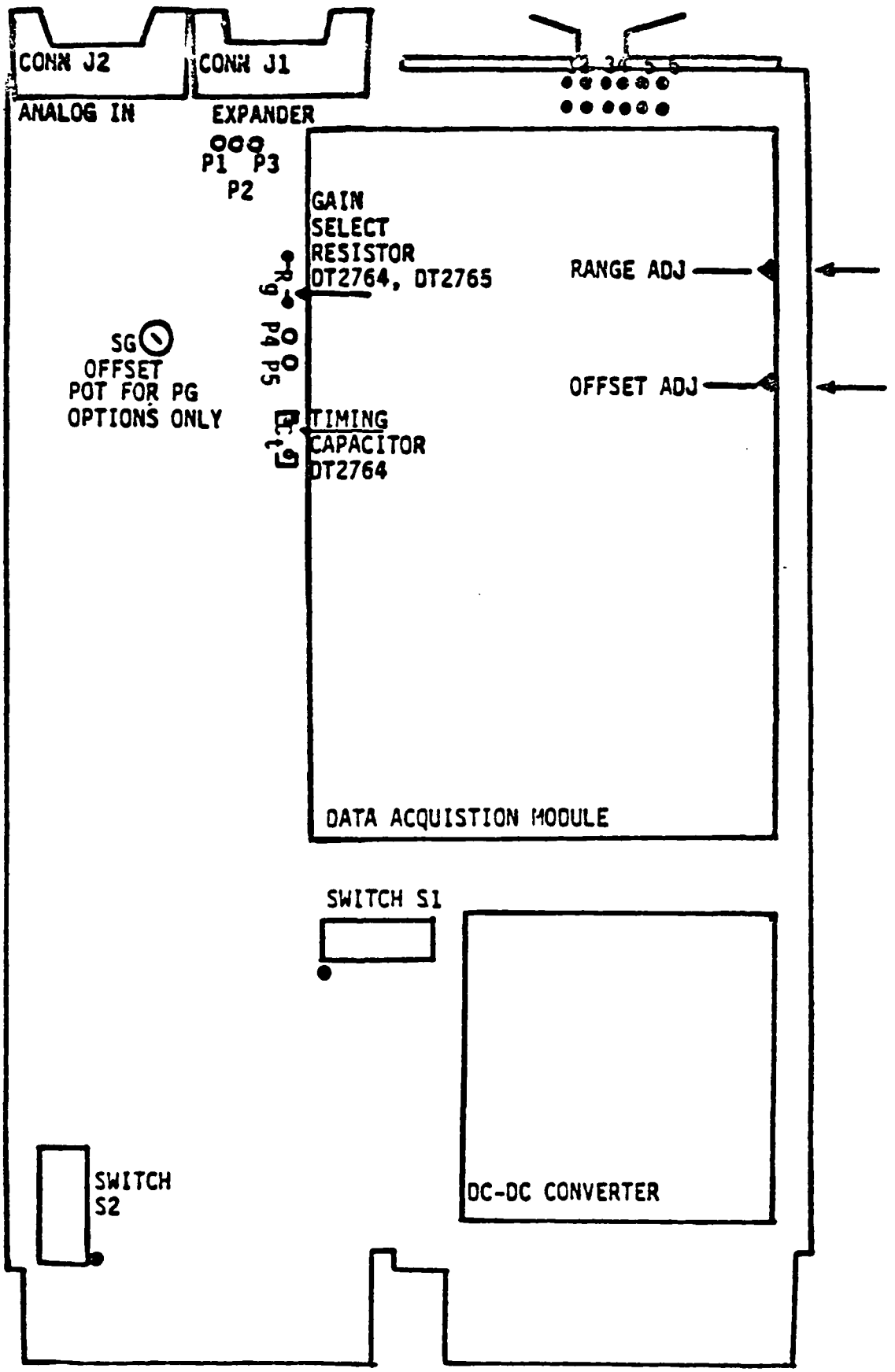


Figure 15. Analog to Digital Converter Module, 1A1A5, Configuration Diagram

High Performance, Economy Strain Gage/RTD Conditioners

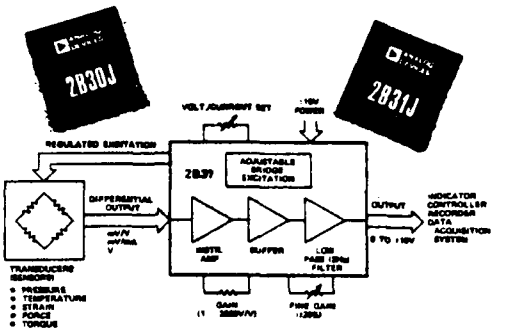
MODELS 2B30 AND 2B31

FEATURES

- Low Cost
- Complete Signal Conditioning Function
- Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
- Wide Gain Range: 1 to 2000V/V
- Low Nonlinearity: 0.0025% max ("L")
- High CMR: 140dB min (60Hz, G = 1000V/V)
- Input Protected to 130V rms
- Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)
- Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100μA to 10mA)

APPLICATIONS

- Measurement and Control of:
  - Pressure, Temperature, Strain/Stress, Force, Torque
- Instrumentation: Indicators, Recorders, Controllers
- Data Acquisition Systems
- Microcomputer Analog I/O



TRANSDUCER SIGNAL CONDITIONING USING 2B31

GENERAL DESCRIPTION

Models 2B30 and 2B31 are high performance, low cost, compact signal conditioning modules designed specifically for high accuracy interface to strain gage-type transducers and RTD's (resistance temperature detectors). The 2B31 consists of three basic sections: a high quality instrumentation amplifier; a three-pole low pass filter, and an adjustable transducer excitation. The 2B30 has the same amplifier and filter as the 2B31, but no excitation capability.

Available with low offset drift of 0.5μV/°C max (RTI, G = 1000V/V) and excellent linearity of 0.0025% max, both models feature guaranteed low noise performance 1μV p-p max, and outstanding 140dB common mode rejection (60Hz, CMV = ±10V, G = 1000V/V) enabling the 2B30/2B31 to maintain total amplifier errors below 0.1% over a 20°C temperature range. The low pass filter offers 60dB/decade roll-off from 2Hz to reduce normal-mode noise bandwidth and improve system signal-to-noise ratio. The 2B31's regulated transducer excitation stage features a low output drift (0.015%/°C max) and a capability of either constant voltage or constant current operation.

Gain, filter cutoff frequency, output offset level and bridge excitation (2B31) are all adjustable, making the 2B30/2B31 the industry's most versatile high-accuracy transducer-interface modules. Both models are offered in three accuracy selections, J/K/L, differing only in maximum nonlinearity and offset drift specifications.

APPLICATIONS

The 2B30/2B31 may be easily and directly interfaced to a wide variety of transducers for precise measurement and control of pressure, temperature, stress, force and torque. For applications in harsh industrial environments, such characteristics as high CMR, input protection, low noise, and excellent temperature stability make 2B30/2B31 ideally suited for use in indicators, recorders, and controllers.

The combination of low cost, small size and high performance of the 2B30/2B31 offers also exceptional quality and value to the data acquisition system designer, allowing him to assign a conditioner to each transducer channel. The advantages of this approach over low level multiplexers include significant improvements in system noise and resolution, and elimination of crosstalk and aliasing errors.

DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The true differential input circuitry with high CMR (140dB) eliminating common-mode noise pickup errors, input filtering minimizing RFI/EMI effects, output low pass filtering (f_c=2Hz) rejecting 50/60Hz line frequency pickup and series-mode noise.

Input and Output Protection: Input protected for shorts to power lines (130V rms), output protected for shorts to ground and either supply.

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

Programmable Transducer Excitation: User-programmable adjustable excitation source-constant voltage (4V to 15V @ 100mA) or constant current (100μA to 10mA) to optimize transducer performance.

Adjustable Low Pass Filter: The three-pole active filter (f_c=2Hz) reducing noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency.

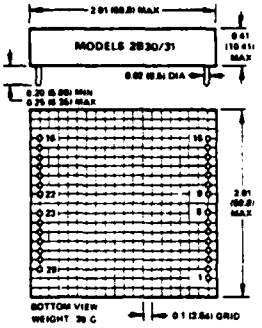
SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

MODEL	2B30J 2B31J	2B30K 2B31K	2B30L 2B31L
GAIN[1]			
Gain Range	1 to 2000V/V	•	•
Gain Equation	$G = (1 + 94k\Omega/R_G) \mid 20k\Omega/(R_P + 16.2k\Omega))$	•	•
Gain Equation Accuracy	±2%	•	•
Fine Gain (Span) Adjust. Range	±20%	•	•
Gain Temperature Coefficient	±25ppm/°C max (±10ppm/°C typ)	•	•
Gain Nonlinearity	±0.01% max	±0.005% max	±0.0025% max
OFFSET VOLTAGES[1]			
Total Offset Voltage, Referred to Input			
Initial, @ +25°C	Adjustable to Zero (±0.5mV typ)	•	•
Warm-Up Drift, 10 Min., G = 1000	±5μV RTI	•	•
vs. Temperature			
G = 1V/V	±150μV/°C max	±75μV/°C max	±50μV/°C max
G = 1000V/V	±3μV/°C max	±1μV/°C max	±0.5μV/°C max
At Other Gains	±(3 ± 150/G)μV/°C max	±(1 ± 75/G)μV/°C max	±(0.5 ± 50/G)μV/°C max
vs. Supply, G = 1000V/V	±25μV/V	•	•
vs. Time, G = 1000V/V	±3μV/month	•	•
Output Offset Adjust. Range	±10V	•	•
INPUT BIAS CURRENT			
Initial @ +25°C	+200nA max (100nA typ)	•	•
vs. Temperature (0 to +70°C)	-0.6nA/°C	•	•
INPUT DIFFERENCE CURRENT			
Initial @ +25°C	±5nA	•	•
vs. Temperature (0 to +70°C)	±40pA/°C	•	•
INPUT IMPEDANCE			
Differential	100MΩ‖47pF	•	•
Common Mode	100MΩ‖47pF	•	•
INPUT VOLTAGE RANGE			
Linear Differential Input	±10V	•	•
Maximum Differential or CMV Input Without Damage	130V rms	•	•
Common Mode Voltage	±10V	•	•
CMR, 1kΩ Source Imbalance			
G = 1V/V, dc to 60Hz[1]	90dB	•	•
G = 100V/V to 2000V/V, 60Hz[1]	140dB min	•	•
dc[3]	90dB min (112 typ.)	•	•
INPUT NOISE			
Voltage, G = 1000V/V			
0.01Hz to 2Hz	1μV p-p max.	•	•
10Hz to 100Hz[2]	1μV p-p	•	•
Current, G = 1000			
0.01Hz to 2Hz	70pA p-p	•	•
10Hz to 100Hz[2]	30pA rms	•	•
RATED OUTPUT[1]			
Voltage, 2kΩ *Load*[3]	±10V min	•	•
Current	±5mA min	•	•
Impedance, dc to 2Hz, G = 100V/V	0.1Ω	•	•
Load Capacitance	0.01μF max	•	•
DYNAMIC RESPONSE (Unfiltered)[2]			
Small Signal Bandwidth			
-3dB Gain Accuracy, G = 100V/V	30kHz	•	•
G = 1000V/V	5kHz	•	•
Slew Rate	1V/μs	•	•
Full Power	15kHz	•	•
Settling Time, G = 100, ±10V Output Step to ±0.1%	30μs	•	•
LOW PASS FILTER (Bessel)			
Number of Poles	3	•	•
Gain (Pass Band)	+1	•	•
Cutoff Frequency (-3dB Point)	2Hz	•	•
Roll-Off	60dB/decade	•	•
Offset (at 25°C)	±5mV	•	•
Settling Time, G = 1000 V/V, ±10V *Output Step to ±0.1%*	600ms	•	•
BRIDGE EXCITATION (See Table 1)			
POWER SUPPLY[4]			
Voltage, Rated Performance	±15V dc	•	•
Voltage, Operating	±(12 to 18)V dc	•	•
Current, Quiescent	±15mA	•	•
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	•	•
Operating	-25°C to +85°C	•	•
Storage	-55°C to +125°C	•	•
CASE SIZE	2" x 2" x 0.4" (51 x 51 x 10.2mm)	•	•

[1] Specifications same as 2B30J/2B31J.
[2] Specifications referred to output at pin 7 with 5.75k, 1%, 25ppm/°C fine span resistor installed and internally set 2Hz filter cutoff frequency.
[3] Specifications referred to the unfiltered output at pin 1.
[4] Protected for shorts to ground and/or either supply voltage.
[5] Recommended power supply: ADI model 902.2 or model 2B35 transducer power supply (for 2B30).
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

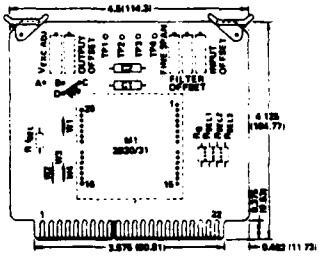


PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1 (UNFILTERED)[1]	16	EXC SEL 1
2	FINE GAIN (SPAN) ADJ	17	I SEL
3	FINE GAIN (SPAN) ADJ	18	$V_{EXC\ OUT}$
4	FILTER OFFSET TRIM	19	$I_{EXC\ OUT}$
5	FILTER OFFSET TRIM	20	SENSE HIGH (+)
6	BANDWIDTH ADJ. 3	21	EXC SEL 2
7	OUTPUT 2 (FILTERED)	22	REF OUT
8	BANDWIDTH ADJ. 2	23	SENSE LOW (-)
9	BANDWIDTH ADJ. 1	24	REGULATOR +V_{IN}
10	R_{GAIN}	25	REF IN
11	R_{GAIN}	26	$-V_S$
12	-INPUT	27	$+V_S$
13	INPUT OFFSET TRIM	28	COMMON
14	INPUT OFFSET TRIM	29	OUTPUT OFFSET TRIM
15	+INPUT		

Note: Pins 10 thru 29 are not connected in Model 2B30

MOUNTING CARDS AC1211, AC1213



AC1211/AC1213 CONNECTOR DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
A	REGULATOR +V_{IN} in	1	EXC SEL 1
B	SENSE LOW (-)	2	I SEL
C	REF OUT	3	$V_{EXC\ OUT}$
D	REF IN	4	$I_{EXC\ OUT}$
E		5	SENSE HIGH (+)
F		6	EXC SEL 2
H		7	OUTPUT OFFSET TRIM
J		8	
K	$-V_S$	9	$-V_S$
L	$+V_S$	10	$+V_S$
M		11	
N	COMMON	12	COMMON
P		13	
R	FINE GAIN ADJ.	14	
S	FINE GAIN ADJ.	15	
T	FILTER OFFSET TRIM	16	
U	FILTER OFFSET TRIM	17	R_{GAIN}
V	OUTPUT 2 (FILTERED)	18	R_{GAIN}
W	- INPUT	19	OUTPUT 1 (UNFILTERED)
X	INPUT OFFSET TRIM	20	BANDWIDTH ADJ. 1
Y	INPUT OFFSET TRIM	21	BANDWIDTH ADJ. 3
Z	+ INPUT	22	BANDWIDTH ADJ. 2

The AC1211/AC1213 mounting card is available for the 2B30/2B31. The AC1211/AC1213 is an edge connector card with pin receptacles for plugging in the 2B30/2B31. In addition, it has provisions for installing the gain resistors and the bridge excitation, offset adjustment and filter cutoff programming components. The AC1211/AC1213 mates with a Cinch 251-22-30-160 (or equivalent) edge connector. The AC1213 includes the adjustment pots; no pots are provided with the AC1211.

FUNCTIONAL DESCRIPTION

Models 2B30 and 2B31 accept inputs from a variety of full bridge strain gage-type transducers or RTD sensors and convert the inputs to conditioned high level analog outputs. The primary transducers providing direct inputs may be 60Ω to 1000Ω strain gage bridges, four-wire RTD's or two- or three-wire RTD's in the bridge configuration.

The 2B30 and 2B31 employ a multi-stage design, shown in Figure 1, to provide excellent performance and maximum versatility. The input stage is a high input impedance ($10^8\Omega$), low offset and drift, low noise differential instrumentation amplifier. The design is optimized to accurately amplify low level (mV) transducer signals riding on high common mode voltages (±10V), with wide (1-2000V/V), single resistor (R_G), programmable gain to accommodate 0.5mV/V to 36mV/V transducer spans and 5Ω to 2000Ω RTD spans. The input stage contains protection circuitry for accidental shorts to power line voltage (130V rms) and RFI filtering circuitry.

The inverting buffer amplifier stage provides a convenient means of fine gain trim (0.8 to 1.2) by using a 10kΩ potentiometer (R_F); the buffer also allows the output to be offset by up to ±10V by applying a voltage to the noninverting input (pin 29). For dynamic, high bandwidth measurements—the buffer output (pin 1) should be used.

The three-pole active filter uses a unity-gain configuration and provides low-pass Bessel-type characteristics-minimum overshoot response to step inputs and a fast rise time. The cutoff frequency (-3dB) is factory set at 2Hz, but may be increased up to 5kHz by addition of three external resistors (R_{SEL_1} - R_{SEL_3}).

INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 illustrates the 2B31 wiring configuration when used in a typical bridge transducer signal conditioning application. A recommended shielding and grounding technique for preserving the excellent performance characteristics of the 2B30/2B31 is shown.

Because models 2B30/2B31 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and conditioner common (pin 28). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains. To avoid ground loops, signal return or cable shield should never be grounded at more than one point.

The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS

Models 2B30/2B31 have been conservatively specified using min-max values as well as typicals to allow the designer to develop accurate error budgets for predictable performance. The error calculations for a typical transducer application, shown in Figure 1 (350Ω bridge, 1mV/V F.S., 10V excitation), are illustrated below.

Assumptions: 2B31L is used, G = 1000, ΔT = ±10°C, source imbalance is 100Ω, common mode noise is 0.25V (60Hz) on the ground return.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources and their effect on system accuracy (worst case) as a % of Full Scale (10V) are listed:

Error Source	Effect on Absolute Accuracy % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.0025	±0.0025
Gain Drift	±0.025	
Voltage Offset Drift	±0.05	
Offset Current Drift	±0.004	
CMR	±0.00025	±0.00025
Noise (0.01 to 2Hz)	±0.01	±0.01
Total Amplifier Error	±0.09175 max	±0.01275 max
Excitation Drift	±0.15 (±0.03 typ)	
Total Output Error (Worst Case)	±0.24175 max (±0.1 typ)	±0.0127 max

The total worst case effect on absolute accuracy over ±10°C is less than ±0.25% and the 2B31 is capable of 1/2 LSB resolution in a 12 bit, low input level system. Since the 2B31 is conservatively specified, a typical overall accuracy error would be lower than ±0.1% of F.S.

In a computer or microprocessor based system, automatic recalibration can nullify gain and offset drifts leaving noise, nonlinearity and CMR as the only error sources. A transducer excitation drift error is frequently eliminated by a ratiometric operation with the system's A/D converter.

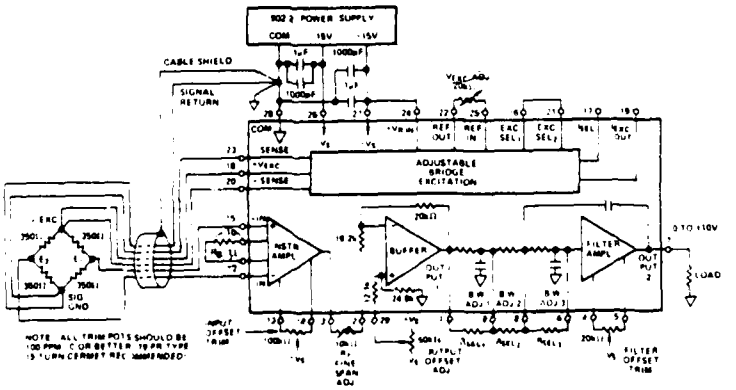


Figure 1. Typical Bridge Transducer Application Using 2B31

BRIDGE EXCITATION (2B31)

The bridge excitation stage of the model 2B31 is an adjustable output, short circuit protected, regulated supply with internally provided reference voltage (+7.15V). The remote sensing inputs are used in the voltage output mode to compensate for the voltage drop variations in long leads to the transducer. The regulator circuitry input (pin 24) may be connected to $+V_S$ or some other positive dc voltage (pin 28 referenced) within specified voltage level and load current range. User-programmable constant voltage or constant current excitation mode may be used. Specifications are listed below in Table 1.

MODEL	2B31J	2B31K	2B31L
Constant Voltage Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	•	•
Output Voltage Range	+4V to +15V	•	•
Regulator Input/Output Voltage Differential	3V to 24V	•	•
Output Current[1]	0 to 100mA max	•	•
Regulation, Output Voltage vs Supply	0.05%/V	•	•
Load Regulation, I_L = 1mA to I_L = 50mA	0.1%	•	
Output Voltage vs Temperature (0 to +70°C)	0.015%/°C max 0.005%/°C typ	• •	• •
Output Noise	1mV rms	•	•
Reference Voltage (Internal)	7.15V ±3%	•	•
Constant Current Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	•	•
Output Current Range	100μA to 10mA	•	•
Compliance Voltage	0 to 10V	•	•
Load Regulation	0.1%	•	•
Temperature Coefficient (0 to +70°C)	0.003%/°C	•	•
Output Noise	1μA rms	•	•

[1] Output Current derated to 33mA max for 24V regulator input/output voltage differential

Table 1. Bridge Excitation Specifications

OPERATING INSTRUCTIONS

Gain Setting: The differential gain, G, is determined according to the equation:

$$G = (1 + 94k\Omega/R_G)\ [20k\Omega/(R_F + 16.2k\Omega)]$$

where R_G is the input stage resistor shown in Figure 1 and R_F is the variable 10kΩ resistor in the output stage. For best performance, the input stage gain should be made as large as possible, using a low temperature coefficient (10ppm/°C) R_G, and the output stage gain can then be used to make a ±20% linear gain adjustment by varying R_F.

Input Offset Adjustment: To null input offset voltage, an optional 100kΩ potentiometer connected between pins 13 and 14 (Figure 1) can be used. With gain set at the desired value, connect both inputs (pins 12 and 15) to the system common (pin 28), and adjust the 100kΩ potentiometer for zero volts at pin 3. The purpose of this adjustment is to null the internal amplifier offset and it is not intended to compensate for the transducer bridge unbalance.

Output Offset Adjustment: The output of the 2B30/2B31 can be intentionally offset from zero over the ±10V range by applying a voltage to pin 29, e.g., by using an external potentiometer or a fixed resistor. Pin 29 is normally grounded if output offsetting is not desired. The optional filter amplifier offset null capability is also provided as illustrated in Figure 1.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency may be increased from the internally set 2Hz by the addition of three external resistors connected as shown in Figure 1. The values of resistors required for a desired cutoff frequency, f_c, above 5Hz are obtained by the equation below:

$$R_{SEL_1} = 11.6 \times 10^6/(2.67f_c - 4.34),$$

$$R_{SEL_2} = 27.6 \times 10^6/(4.12f_c - 7)$$

$$R_{SEL_3} = 1.05 \times 10^6/(0.806f_c - 1.3)$$

where R_{SEL} is in ohms and f_c in Hz. Table 2 gives the nearest 1% R_{SEL} for several common filter cutoff (-3dB) frequencies.

f_c (Hz)	R_{SEL1} (kΩ) (Pin 1 to 9)	R_{SEL2} (kΩ) (Pin 9 to 8)	R_{SEL3} (kΩ) (Pin 8 to 6)
2	Open	Open	Open
5	1270.000	2050.00	383.000
10	523.000	806.00	154.000
50	90.000	137.00	26.700
100	44.200	68.10	13.300
500	8.660	13.30	2.610
1000	4.320	6.65	1.300
5000	0.866	1.33	0.261

Table 2. Filter Cutoff Frequency vs. R_{SEL}

Voltage Excitation Programming: Pin connections for a constant voltage output operation are shown in Figure 2. The bridge excitation voltage, V_{EXC}, is adjusted between +4V to +15V by the 20kΩ (50ppm/°C) R_{VSEL} potentiometer. For ratiometric operation, the bridge excitation can be adjusted by applying an external positive reference to pin 25 of the 2B31. The output voltage is given by: $V_{EXC\ OUT} = 3.265V_{REF\ IN}$. The remote sensing leads should be externally connected to the excitation leads at the transducer or jumpered as shown in Figure 2 if sensing is not required.

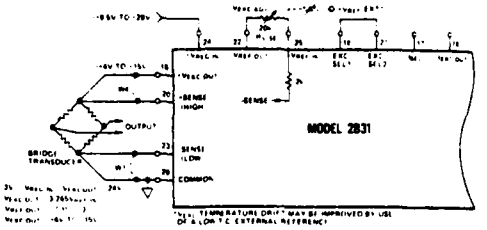


Figure 2. Constant Voltage Excitation Connections

Current Excitation Programming: The constant current excitation output can be adjusted between 100μA to 10mA by two methods with the 2B31. Figure 3 shows circuit configuration for a current output with the maximum voltage developed across the sensor (compliance voltage) constrained to +5V. The value of programming resistor R_{ISEL} may be calculated from the relationship: $R_{ISEL} = (V_{REG\ IN} - V_{REF\ IN})/I_{EXC\ OUT}$

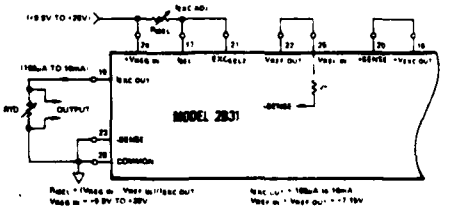


Figure 3. Constant Current Excitation Connections (V_{COMPL} = 0 to +5V)

A compliance voltage range of 0 to +10V can be obtained by connecting the 2B31 as shown in Figure 4. The 2kΩ potentiometer R_{ISEL} is adjusted for desired constant current excitation output.

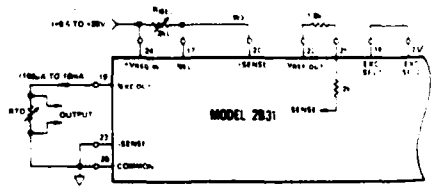


Figure 4. Constant Current Excitation Connections (V_{COMPL} = 0 to +10V)

APPLICATIONS

Strain Measurement: The 2B30 is shown in Figure 5 in a strain measurement system. A single active gage (120Ω, GF = 2) is used in a bridge configuration to detect small changes in gage resistance caused by strain. The temperature compensation is provided by an equivalent dummy gage and two high precision 120Ω resistors complete the bridge. The 2B35 adjustable power supply is set to a low +3V excitation voltage to avoid the self-heating error effects of the gage and bridge elements. System calibration produces a 1V output for an input of 1000 microstrains. The filter cutoff frequency is set at 100Hz.

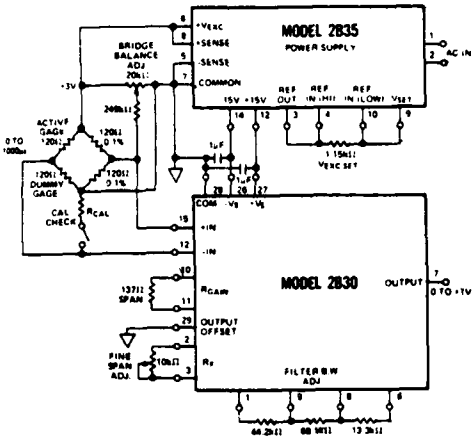


Figure 5. Interfacing Half-Bridge Strain Gage Circuit

Pressure Transducer Interface: A strain gage type pressure transducer (BLH Electronics, DHF Series) is interfaced by the 2B31 in Figure 6. The 2B31 supplies regulated excitation (+10V) to the transducer and operates at a gain of 333.3 to achieve 0-10V output for 0-10,000 p.s.i. at the pressure transducer. Bridge Balance potentiometer is used to cancel out any offset which may be present and the Fine Span potentiometer adjustment accurately sets the full scale output. Depressing the calibration check pushbutton switch shunts a system calibration resistor (R_{CAL}) across the transducer bridge to give an instant check on system calibration.

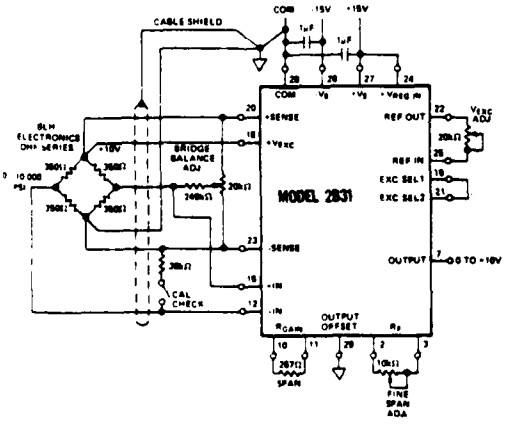


Figure 6. Pressure Transducer Interface Application

Platinum RTD Temperature Measurement: In Figure 7 model 2B31 provides complete convenient signal conditioning in a wide range (-100°C to +600°C) RTD temperature measurement system. YSI - Sostman four-wire, 100Ω platinum RTD (PT139AX) is used. The four wire sensor configuration, combined with a constant current excitation and a high input impedance offered by the 2B31, eliminates measurement errors resulting from voltage drops in the lead wires. Offsetting may be provided via the 2B31's offset terminal. The gain is set by the gain resistor for a +10V output at +600°C.

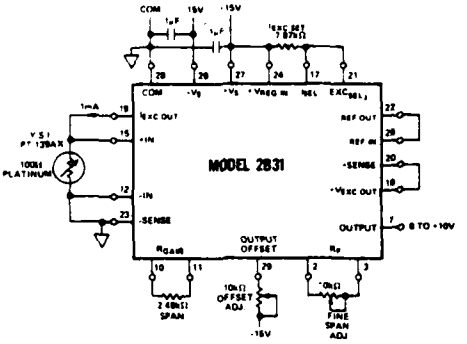


Figure 7. Platinum RTD Temperature Measurement

Interfacing Three-Wire Sensors: A bridge configuration is particularly useful to provide offset in interfacing to a platinum RTD and to detect small, fractional sensor resistance changes. Lead compensation is employed, as shown in Figure 8, to maintain high measurement accuracy when the lead lengths are so long that thermal gradients along the RTD leg may cause changes in line resistance. The two completion resistors (R1, R2) in the bridge should have a good ratio tracking (±5ppm/°C) to eliminate bridge error due to drift. The single resistor (R3) in series with the platinum sensor must, however, be of very high absolute stability. The adjustable excitation in the 2B31 controls the power dissipated by the RTD itself to avoid self-heating errors.

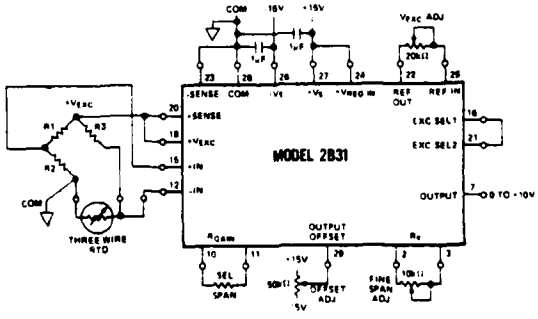


Figure 8. Three-Wire RTD Interface

Linearizing Transducer Output: To maximize overall system linearity and accuracy, some strain gage-type and RTD transducer analog outputs may require linearization. A simple circuit may be used with the 2B31 to correct for the curvature in the input signal. Consult factory for the application assistance.

Data Acquisition System: Figure 9 shows a typical application of the 2B30/2B31 in a low level, high speed microcomputer based data acquisition system. The advantages of this configuration are improvement in CMR enhanced by a low pass filter/channel provided by the 2B31, elimination of aliasing errors and crosstalk noise between input channels, improvement in system noise and resolution, and optimized, individual bridge excitation source for each channel.

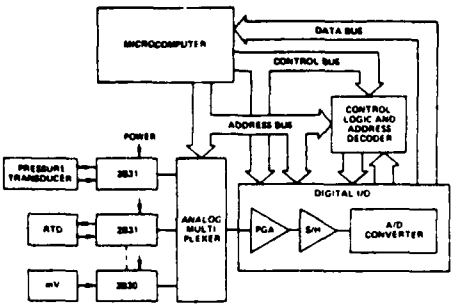


Figure 9. Use of the 2B30/2B31 in Data Acquisition System

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Models 2B30/2B31 are available in three drift selections: ±0.5, ±1 and ±3μV/°C (max, RTI, G = 1000V/V). Total input drift is composed of two sources (input and output stage drifts) and is gain dependent. Figure 10 is a graph of the worst case total voltage offset drift vs. gain for all versions.

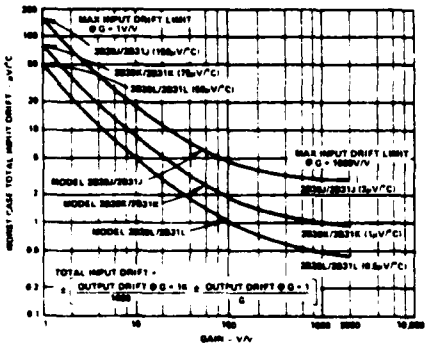


Figure 10. Total Input Offset Drift (Worst Case) vs. Gain

Gain Nonlinearity and Noise: Nonlinearity is specified as a percent of full scale (10V), e.g. 0.25mV RTO for 0.0025%. Three maximum nonlinearity selections offered are: ±0.0025%, ±0.005% and ±0.01% (G = 1 to 2000V/V). Models 2B30/2B31 offer also an excellent voltage noise performance by guaranteeing maximum RTI noise of 1μV p-p (G = 1000V/V, $R_S \leq 5k\Omega$) with noise bandwidth reduced to 2Hz by the low pass filter

Low Pass Filter: The three pole Bessel-type active filter attenuates unwanted high-frequency components of the input signal above its cutoff frequency (-3dB) with 60dB/decade rolloff. With a 2Hz filter, attenuation of 70dB at 60Hz is obtained, settling time is 600ms to 0.1% of final value with less than 1% overshoot response to step inputs. Figure 11 shows the filter response

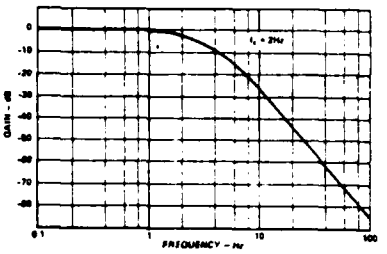


Figure 11. Filter Amplitude Response vs. Frequency

Common Mode Rejection: CMR is rated at ±10V CMV and 1kΩ source imbalance. The CMR improves with increasing gain. As a function of frequency, the CMR performance is enhanced by the incorporation of low pass filtering, adding to the 90dB minimum rejection ratio of the instrumentation amplifier. The effective CMR at 60Hz at the output of the filter (f_c = 2Hz) is 140dB min. Figure 12 illustrates a typical CMR vs. Frequency and Gain.

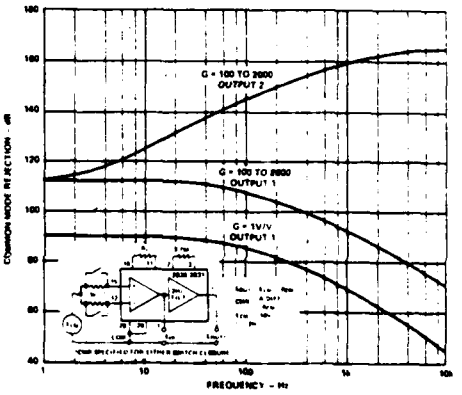


Figure 12. Common Mode Rejection vs. Frequency and Gain

Bridge Excitation (2B31): The adjustable bridge excitation is specified to operate over a wide regulator input voltage range (+9.5V to +28V). However, the maximum load current is a function of the regulator circuit input-output differential voltage, as shown in Figure 13. Voltage output is short circuit protected and its temperature coefficient is ±0.015% V_{OUT}/°C max (±0.003%/°C typ). Output temperature stability is directly dependent on a temperature coefficient of a reference and for higher stability requirements, a precision external reference may be used.

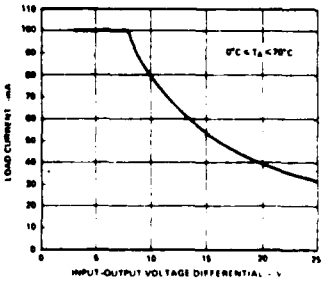


Figure 13. Maximum Load Current vs. Regulator Input-Output Voltage Differential

MATH ASSOCIATES, INC.

2200 Shames Drive. Westbury. NY 11590 • 516-334-6800

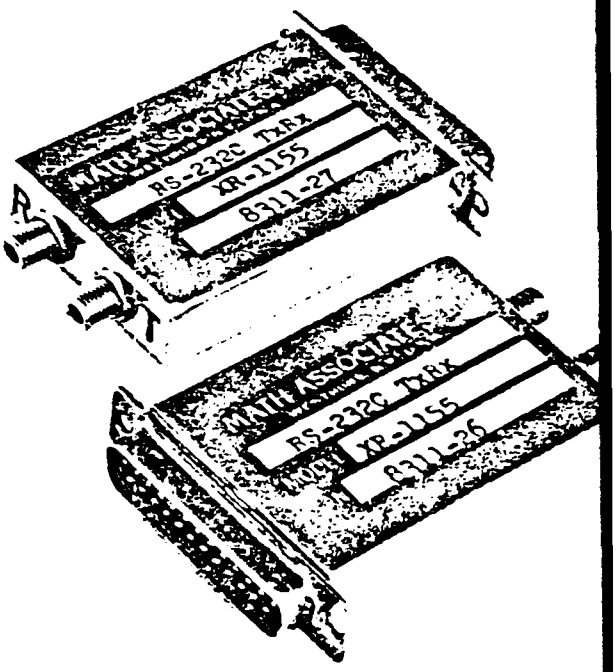
OPERATING INSTRUCTIONS

XR-1150/55 RS232-C DATA TRANSMISSION SYSTEM

INTRODUCTION

The FIBERLINK XR-1150/55 RS232-C Data Transmission System is a fully solid state "optical modem" that will enable error-free data to be transmitted via fiber optics over distances exceeding a mile.

It is ideal for extending the normal transmission range of computers, microprocessors, keyboards, terminals, and other RS232-C compatible equipment and accessories. The XR-1150/55 may be used in either a DCE or DTE mode as switch selected by the user.



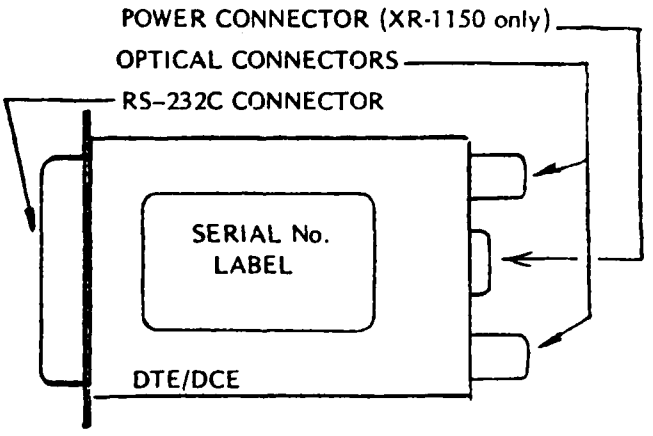
SPECIFICATIONS

DATA TRANSMISSION RATE		DC to 100Kbits/sec
OPERATING MODE		Simplex, Full Duplex,
LOGICAL "1" INPUT/OUTPUT		+3.75V to +10VDC
LOGICAL "0" INPUT/OUTPUT		−3.75V to −10VDC
ALLOWABLE OPTICAL ATTENUATION		25dB
OPERATING WAVELENGTH		820nm
OPTICAL CONNECTORS		SMA
ELECTRICAL CONNECTOR		EIA compatible DB-25P
POWER REQUIREMENTS	XR-1150	12VDC @250ma*
	XR-1155	±12 to ±15VDC @100ma
OPERATING TEMPERATURE RANGE		0 to 50°C

*Obtained from XP-1150 plug-in AC adaptor

FUNCTIONAL DESCRIPTION

The drawing below indicates the various parts of the XR-1150/55 that the user will be concerned with in normal use.



USING THE XR-1150/55

Using the XR-1150/55 requires simply selecting the DCE or DTE mode, plugging the two units into the RS232-C ports, attaching the fiber optic cable, and supplying power. There are some considerations however which must be met.

2732A
32K (4K x 8) UV ERASABLE PROM

- 200 ns (2732A-2) Maximum Access Time . . . HMOS*-E Technology
- Compatible to High Speed 8 MHz 8086-2 MPU . . . Zero WAIT State
- Two Line Control
- Pin Compatible to 2764 EPROM
- Industry Standard Pinout . . . JEDEC Approved
- Low Standby Current . . . 35 mA Maximum
- ±10% V_{CC} Tolerance Available

The Intel* 2732A is a 5V only, 32,768 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). It is pin compatible to Intel's 450 ns 2732. The standard 2732A's access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible to high performance microprocessors, such as the 8 MHz 8086-2. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

An important 2732A feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 2732A has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 125 mA, while the maximum standby current is only 35 mA, a 70% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The 2732A is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

*HMOS is a patented process of Intel Corporation

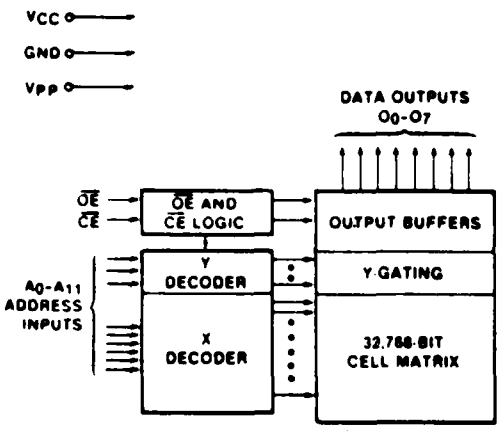
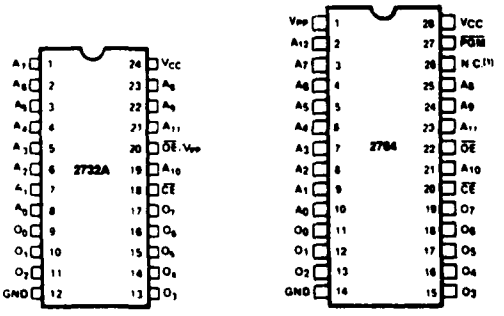


Figure 1. Block Diagram

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS



[1] For upgradability to JEDEC approved 128K EPROMs, provide an address line to pin 26. For compatibility with the 2732A and 32K ROMs, provide a trace from V_{CC} to pin 26

Figure 2. Pin Configurations

ERASURE CHARACTERISTICS

The erasure characteristics of the 2732A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2732A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2732A window to prevent unintentional erasure.

The recommended erasure procedure for the 2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000μW/cm^2 power rating. The 2732A should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The 2732A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The 2732A has a standby mode which reduces the active power current from 125 mA to 35 mA. The 2732A is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING (See Programming Instruction Section for Waveforms.)

Programming is the same as Intel's 450 ns 2732 except for the programming voltage. In the program mode the 2732A $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 21V (25V for the 2732). ***Exceeding 22V will damage the 2732A.***

Initially, and after each erasure, all bits of the 2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time —either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple 2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732As may be common. A TTL level program pulse applied to a 2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that 2732A. A high level $\overline{CE}$ input inhibits the other 2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

System Consideration

The power switching characteristics of HMOS-E EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, as detailed in Intel's Application Note, AP-72, and/or by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board-traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... +6V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming ..... +22V to −0.3V

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC AND AC OPERATING CONDITIONS DURING READ

	2732A/A-2/A-3/A-4	2732A-20/A-25/A-30
Operating Temperature Range	0°C–70°C	0°C–70°C
V_{CC} Power Supply	5V ± 5%	5V ± 10%

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.5V
I_{CC1}	V_{CC} Current (Standby)			35	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)			125	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

A.C. CHARACTERISTICS

Symbol	Parameter	2732A-2 2732A-20		2732A 2732A-25		2732A-3 2732A-30		2732A-4		Units	Test Conditions*
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{ACC}	Address to Output Delay		200		250		300		450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300		450	ns	$\overline{OE}$ = V_{IL}
t_{OE}	$\overline{OE}$ to Output Delay		70		100		150		150	ns	$\overline{CE}$ = V_{IL}
t_{DF}[2]	$\overline{OE}$ High to Output Float	0	60	0	90	0	130	0	130	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

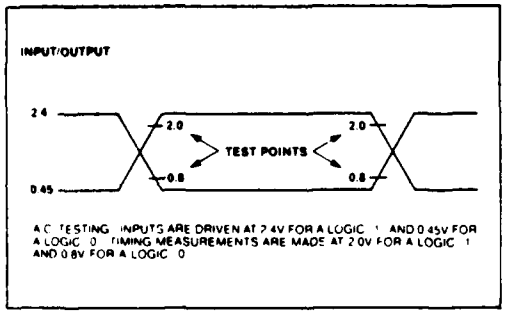
*A.C. TEST CONDITIONS

Output Load ..... 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times ..... ≤ 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs ..... 0.8 and 2.0V
Outputs ..... 0.8 and 2.0V

CAPACITANCE[2] (T_A = 25°C, f = 1 MHz)

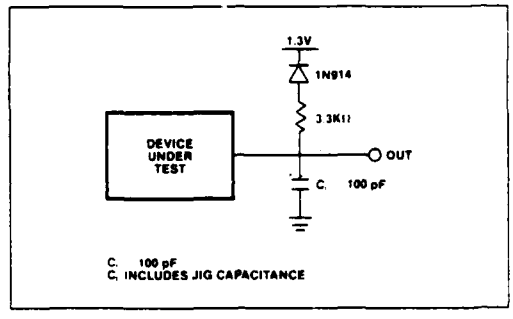
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TESTING INPUT, OUTPUT WAVEFORM



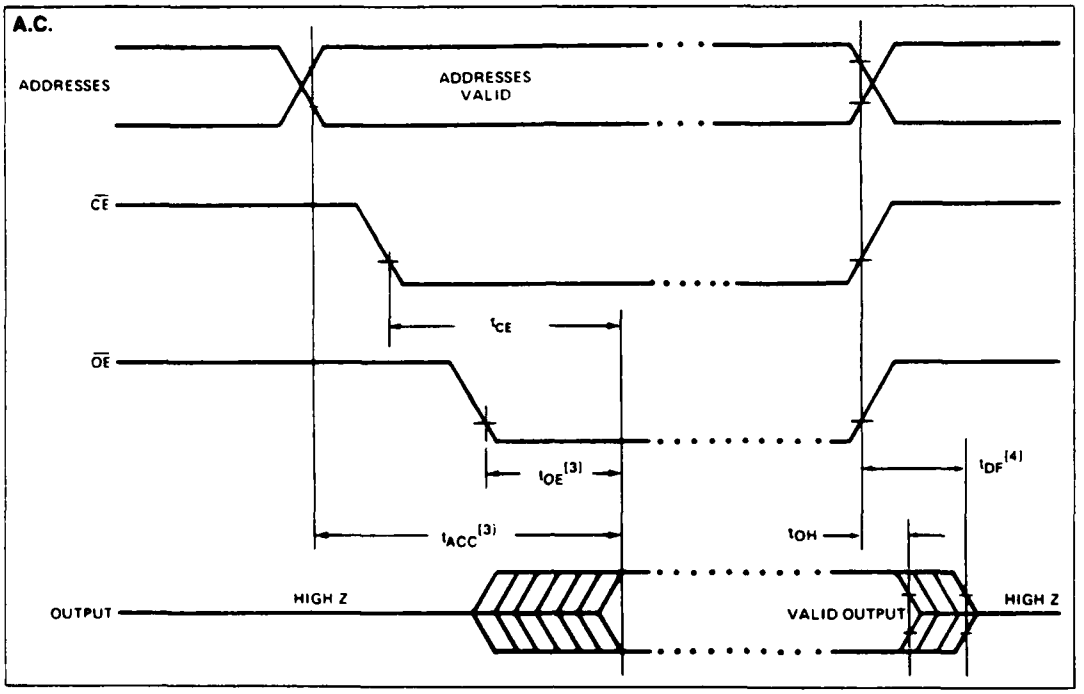
A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L INCLUDES JIG CAPACITANCE

WAVEFORM



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS[5] (T_A = 25 ± 5°C, V_{CC} = 5V ± 5%, V_{PP} = 21V ± 0.5V)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output Low Voltage During Verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4			V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		85	125	mA	
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except OE/V_{PP})	2.0		V_{CC} + 1	V	
I_{PP}	V_{PP} Supply Current			35	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

NOTE:
5. When programming the 2732A, a 0.1 μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

A.C. PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5V ± 5%, V_{PP} = 21V ± 0.5V)

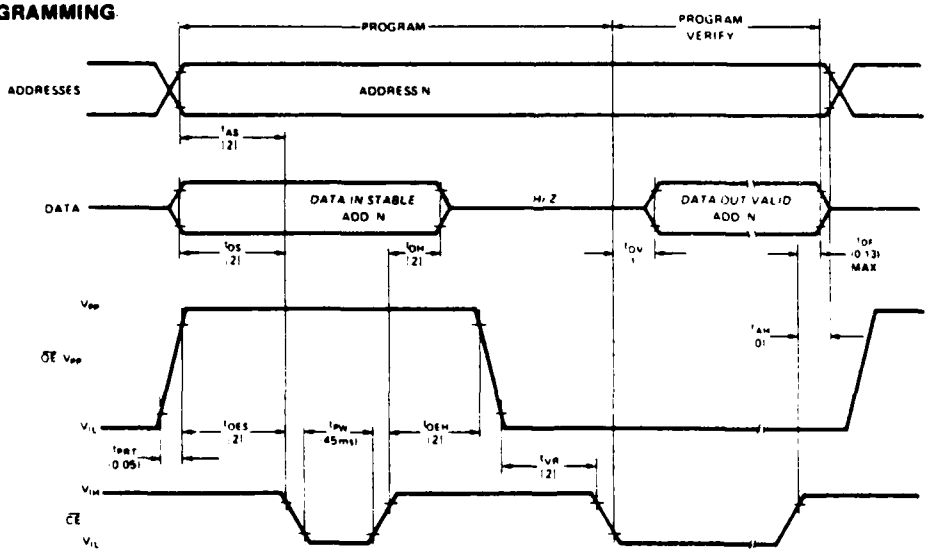
Symbol	Parameter	Limits			Units	Test Conditions†
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{OEH}	OE Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Enable to Output Float Delay	0		130	ns	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
t_{PW}	$\overline{CE}$ Pulse Width During Programming	45	50	55	ms	
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			μs	

†A.C. TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 1.0 and 2.0V
Output Timing Reference Level ..... 0.8 and 2.0V

WAVEFORM

PROGRAMMING



1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED
2. THE INPUT TIMING REFERENCE LEVEL IS 1V FOR A V_{IL} AND 2V FOR A V_{IH}

AFN-01545B

APPENDIX B - PARTS LIST

APPENDIX B - PARTS LIST

Reference Designation	Material/Description	Quantity
1	System enclosure	1 ea
	SB-8-NFP pack mounted chassis kit	1 ea
	Hinged front panel for above	1 ea
1A1	H9281-BC 2x12 slot backplane	1 ea
1A1A1	KDF11-AA LSI-11/23 microcomputer module	1 ea
	DEF11-A LSI-11/23 floating paint option	
1A1A2	KWV11-C programmable real-time clock module	1 ea
1A1A3	MXV11-AC multifunction module	1 ea
1A1A4	MRV11-C 32 K EPROM module	1 ea
1A1A4	32 Kx.8 EPROMs 250 nsec 2732A (Intel)	16 ea
1A1A5	DT2762-DI high level, A/D converter, 8-channel	1 ea
1A1A6	AAV11-C 4-channel D/A converter module	1 ea
1A1A7	DRV-11 parallel line interface module	1 ea
1A1A8	W984 dual extender card	1 ea
1A2	Discrete input interface board	1 ea
	PC board	1 ea
	LM-340-5 regulator	1 ea
	74LS04 hex gate	2 ea
	5 K, 1/8 W composition resistor	12 ea
	0.22 mf capacitor	1 ea
	0.1 mf capacitor	1 ea
	0.01 mf capacitor	2 ea
1A3	Cooling fan	
1F1	Fuse, 15A	1 ea
1F1-1F4	Fuse holder	4 ea
1F2-1F4	Fuses, 1A	3 ea
1FL1	10VB1 RFI filter	1 ea
1P1	Power receptacle	1 ea
1P2,1P3	Power outlet	1 ea
1P4	3-contact box mounting receptacle	1 ea
1P5,1P6	DB-255 ribbon cable connector	2 ea
1PS1	H780-H master power supply	1 ea
1PS2	HBB15-1, 5A power supply	1 ea
	OVP-12 overvoltage protection	1 ea
1S1	Power switch	1 ea
1S2	28F2000 power tap switch	1 ea
1S3	82601 toggle switch	1 ea
1S4,1S5	JMT-127 toggle switch	2 ea
1TB1	3-contact terminal block	1 ea
1TB2	8-contact terminal block	1 ea
2	19"x8.75"x0.125" aluminum panel	1 ea
2A1-2A4	1583 031 22134 200 44-contact edge connector	4 ea
	Strain gauge conditioner boards	4 ea
	2B31K, strain gauge conditioner	4 ea
	AC1211, mounting card for 2B31K	4 ea
	274 ohm precision resistor (R6)	4 ea
	2150 ohm precision resistor (R3)	4 ea
	3320 ohm precision resistor (R5)	4 ea
	649 ohm precision resistor (R4)	4 ea

Reference Designation	Material/Description	Quantity
2A5-2A8	Servodriver boards	4 ea
	AD380JH op. amp.	4 ea
	10 pf capacitor CD10J 300 V (C1,C2)	8 ea
	1 mf capacitor x440 (C3,C4)	8 ea
	10 mf capacitor 10-50 (C5,C6)	8 ea
	10 K potentiometer 680X (R1)	4 ea
	100 K resistor 5% 1/8 W (R3)	4 ea
	1270 ohm precision resistor (R2)	4 ea
	Servodriver PC board	4 ea
	50-6A-20 6-contact edge connector	4 ea
2A1-2A8	33-9016-12-01-04 PC card guides	16 ea
2P1-2P8	DB-25P connectors	8 ea
2TB1-2TB6	12-contact terminal block	6 ea
3A1,3A2	XR-1150 RS-232 transceiver	2 ea
W1	Power cord	1 ea
W2	PT06A-8-3P 3-contact straight plug	1 ea
	3-conductor 22 gauge cable	10 ft
W3,W4	ADF-100-2 fiber-optic cable	1 ea
	SMA connector termination for above cable	4 ea
W5,W6	DB-25S ribbon cable connector	4 ea
	20-contact header connector	2 ea
	20-conductor ribbon cable	50 ft
W7,W8	DB-25P connector	4 ea
	40 conductor ribbon cable	50 ft
	TP 221 E04 44 contact edge connector	2 ea
	40 contact head connector	2 ea
W9,W10	BCZON-05 null modem cable	2 ea
W11,W12	XR-1150 AC adapter	2 ea

U.S. GPO 559-065

END

FILMED

11-85

DTIC